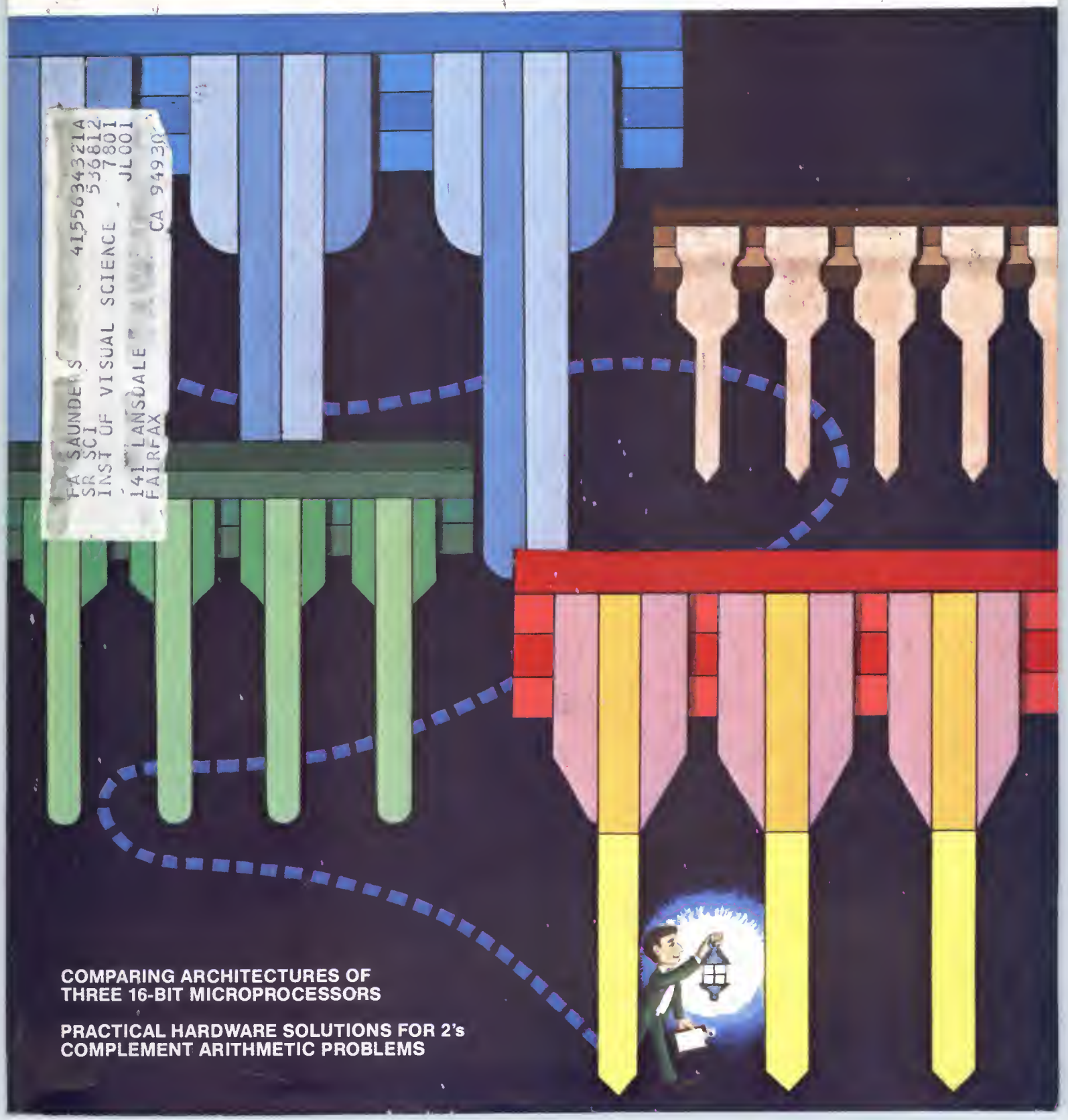
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JULY 1979



COMPARING ARCHITECTURES OF THREE 16-BIT MICROPROCESSORS

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COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JULY 1979

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BPA **CIRCULATION: 67,155 (JUNE 1978)**

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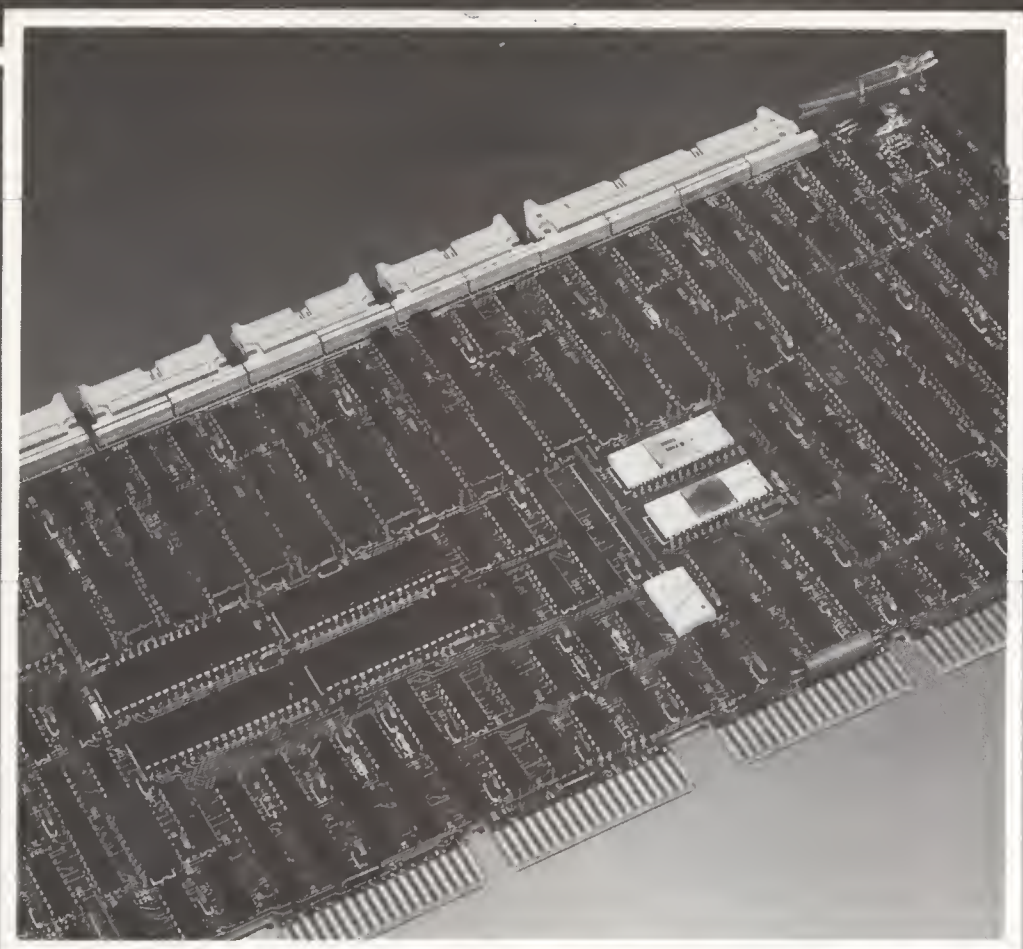

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LETTERS TO THE EDITOR

To the Editor:

I was extremely pleased to read Mr B. E. Forbes' article: "IEEE 488: A Proposed Microcomputer I/O Bus Standard" (*Computer Design*, Nov 1978, pp 170-174). Not only was it well written, but also I fully agreed with all the points raised.

I would, however, like to comment on another characteristic of the GPIB, namely the CPU to CPU link. The IEEE Std 488 does have the capability to get, pass, and take control from other controllers. As such, many of the issues of control-transfer are answered. However, the REN and IFC messages can be issued only by the System-Controller. Unfortunately, the IEEE 488 does not provide a Take-System-Control message. The RSC message is local and a human operator should select the right device to possess the system control virtue. This is a shortcoming and seems artificial and not inherently necessary.

M. Guttman
Elta Electronics Industries Ltd
New York, NY

To the Editor:

We enjoyed the March 1979 article in *Computer Design* on "Comparison of Selected Array Processor Architectures" by S. P. Hufnagel (pp 151-158). We agree with Mr Hufnagel that for most applications the ideal maximum rate cannot be achieved, except for short bursts of time. However, there are realistic applications of practical importance that can drive an array processor to the ideal maximum rate most of the time. Here at the Fusion Div of the General Atomic Co, we are operating the world's largest tokamak, the Doublet III machine, for fusion energy research. One of the major goals of Doublet III is to maintain and confine a hot (tens of million degrees) ionized gas (plasma) in a peanut-shaped cross-section utilizing external magnetic fields. The theoretical studies and the interpretation of experimental results require repeated solution of a free-boundary nonlinear partial differential equation which describes the magneto-hydrodynamic equilibrium of the plasma. This Poisson-like differential equation can be solved by using the standard Green's function method. The major portion of the computation is simply of the form $\psi_i = \Sigma M_{ij} I_j$ where ψ_i is the magnetic flux, I_j is the plasma current, and M_{ij} is the mutual inductance matrix. The vector length of ψ and I is of the order of 1500. By storing I_j in RAM table memory and M_{ij} in main data memory, we are able to drive our DECsystem 10-AP190L to the ideal of 12M flops performing the matrix multiplication as a series of dot products as shown above. A typical solution takes approximately 11 s on our array processor. As a comparison, the same problem takes 8 s on a CDC 7600 and 3.2 s on a CRAY-1. We estimate that the array processor is running at its ideal maximum rate at least 60% of the 11 s.

T. S. Wang, M. Saito, S. Karin
General Atomic Co
San Diego, Calif

To the Editor:

The Project Management Institute is conducting a survey of scheduling software systems available and on the market today. We would like to contact software vendors who wish to participate in this survey.

The Project Management Institute is identifying as many CPM scheduling software packages or related programs (MIS, cost control, material control, etc) as possible that are currently available to project managers or owners for their use either through purchase, lease, or service bureau arrangements.

Any firms, software vendors, or individuals that wish to participate or have their packages included, please contact Ozro E. West, 2329 Laguna St, San Francisco, CA 94115, 415/567-3232. Standardized information questionnaries will be sent to all who request and when completed, will be published in a bound volume for purchase. A copy of the survey results can be obtained by contacting the Project Management Institute, PO Box 43, Drexel Hill, PA 19026.

PMI is interested in all project control related programs, particularly those recently developed, current enhancements to programs that have been available for many years, or packages developed for use on minicomputers.

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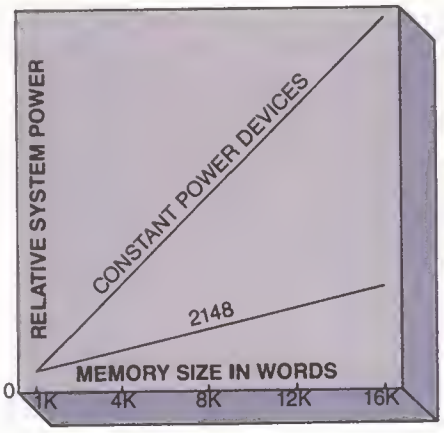

it's the same process we use to produce our industry standard 16-bit microcomputer, the 8086.

Intel has already delivered over 7 million HMOS RAMs. This gives 2148 users a proven track record of reliability and volume availability. For more detailed information on HMOS dependability, request our comprehensive HMOS Reliability Report #18.

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	2148-3	2148	2148-6
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Max. Standby Current (mA)	30	30	30

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*HMOS is a patented Intel process.

CALENDAR

CONFERENCES

AUG 6-8—Pattern Recognition and Image Processing, Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: PRIP 79, PO Box 639, Silver Spring, MD 20901

AUG 13-15—Conf on Simulation, Measurement, and Modeling of Computer Systems, Boulder, Colo. INFORMATION: Paul F. Roth, National Bureau of Standards, Technology Bldg, Rm B-250, Washington, DC 20234

AUG 19-22—Rocky Mountain Symp on Microcomputers, Pingree Park, Colo. INFORMATION: Michael Tindall, Dept of Computer Science, Colorado State U, Fort Collins, CO 80523

AUG 21-24—Internat'l Conf on Parallel Processing, Shanty Creek Lodge, Bellaire, Mich. INFORMATION: 1979 Internat'l Conf on Parallel Processing, Dept of Electrical and Computer Engineering, Wayne State U, Detroit, MI 48202

SEPT 4-7—COMPCON, Washington, DC. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901

SEPT 5-7—Internat'l Fiber Optics and Communications Exposition, Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: Michael A. O'Bryant, Director, Expositions and Publications, Information Gatekeepers, Inc, 167 Carey Rd, Suite 111, Brookline, MA 02146. Tel: 617/739-2022

SEPT 7-9—Internat'l Microcomputer Exposition, Dallas, Tex. INFORMATION: IME, 413 Carillon Tower, 13601 Preston Rd, Dallas, TX 75240

SEPT 18-21—WESCON, Brooks Hall and St Francis Hotel, San Francisco, Calif. INFORMATION: William C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

SEPT 19-21—Internat'l Automatic Testing Conf, Radisson Hotel, Minneapolis, Minn. INFORMATION: A. O. Thornsjo, Honeywell Inc, 1625 Zarthan Ave S, St Louis Park, MN 55416. Tel: 612/542-4811

SEPT 20-26—TELCOM '79, Geneva, Switzerland. INFORMATION: John Sodalski, 2001 Eye St NW, Washington, DC 20006. Tel: 202/457-4934

SEPT 25-27—Mini/Micro Computer Conf and Expo, Anaheim, Calif. INFORMATION: Robert D. Rankin, 5528 E LaPalma Ave, Suite 1, Anaheim, CA 92807

SEPT 26-29—Mini and Microcomputers Internat'l Symp and Exhibition, Queen Elizabeth Hotel, Montreal, Canada. INFORMATION: The Secretary, MIMI '79, PO Box 2481, Anaheim, CA 92804. Tel: 714/774-6144

SEPT 28-30—Northeast Personal and Business Computer Show, Hynes Auditorium/Prudential Ctr, Boston, Mass. INFORMATION: Northeast Expositions, PO Box 678, Brookline Village, MA 02147. Tel: 617/522-4467

OCT 2-4—Internat'l Electrical, Electronics Conf and Exposition, Exhibition Place, Toronto, Canada. INFORMATION: Internat'l Electrical, Electronics Conf and Exposition, 1450 Don Mills Rd, Don Mills, Ontario M3B 2X7, Canada

OCT 2-5—Internat'l Conf on Distributed Computing Systems, Huntsville, Ala. INFORMATION: B. D. Carroll, Electrical Engineering, Auburn U, 207 Dunstan Hall, Auburn, AL 36830. Tel: 205/826-4330

OCT 3-5—Internat'l Conf on Very Large Data Bases, National Hotel, Rio De Janeiro, Brazil. INFORMATION: Prof Stanley Y. W. Su, 500 A Weil Hall, U of Florida, Gainesville, FL 32611. Tel: 904/392-2371

OCT 8-9—Symp on Hardware Descriptive Languages, Palo Alto, Calif. INFORMATION: Waldo Magnusan, Lawrence Livermore Labs, PO Box L-156, Livermore, CA 94550. Tel: 415/422-9550

OCT 9-11—Compusign, Anaheim, Calif. INFORMATION: Golden Gate Enterprises, Inc, 1307 S Mary Ave, Suite 210, Sunnyvale, CA 94087. Tel: 408/735-1122

OCT 14-17—Electronic and Aerospace Systems Convention (EASCON), Stouffer's Inn, Washington, DC. INFORMATION: William C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

OCT 22-24—Computers in Aerospace Conf, Hyatt House Hotel, Los Angeles, Calif. INFORMATION: Richard R. Erkeneff, McDonnell Douglas Astronautics Co, Dept 236, Bldg 13-3, 5301 Balsa Ave, Huntington Beach, CA 92644. Tel: 714/896-4975

OCT 23-25—European Symp on Realtime Data Handling and Process Control, West Berlin, Germany. INFORMATION: Real-Time Data 79, Congress Organization Co, Kongress Zentrale, John Foster Dulles Allee 10, D-1000 Berlin 21, Germany

OCT 23-25—Semiconductor Test Conf, Hyatt House, Cherry Hill, NJ. INFORMATION: Tess Mitchell, Secretary/Registrar, PO Box 38, Collegeville, PA 19426. Tel: 215/489-9387

OCT 29-31—Symp on Foundations of Computer Science, San Juan, Puerto Rico. INFORMATION: Prof Ronald V. Book, Dept of Math and Computer Science, U of California, Santa Barbara, CA 93106. Tel: 805/961-2778

OCT 30-31—Interface West, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

NOV 6-8—COMPEC Peripherals, Systems, and Mini and Microcomputer Specialized Exhibition, Olympia Grand Hall, London, England. INFORMATION: Iliffe Promotions Ltd, Dorset House, Stamford St, London SE1 9LU, England

SHORT COURSES

AUG 13-17—Computer Image Processing, Rensselaer Polytechnic Institute, Troy, NY. INFORMATION: Richard J. Teich, Office of Continuing Studies, Rensselaer Polytechnic Institute, Troy, NY 12181. Tel: 518/270-6442

AUG 20-22—Digital Communications Processing and Coding, and SEPT 12-14—Computer Programming for the Nonprogrammer, George Washington U, Washington, DC. INFORMATION: Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: 202/676-6106

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COMMUNICATION CHANNEL

TRENDS IN THE DIGITAL TRANSMISSION OF VOICE AND IMAGE SIGNALS— PART 1: VOICE DIGITIZATION

Ira Richer

Bolt Beranek and Newman Incorporated
Cambridge, Massachusetts

There are several different kinds of reasons for wanting to digitize analog signals in a communications environment. Digital signals are compatible with computers and can be stored and processed in convenient and sophisticated ways; they can be communicated economically by reducing the bandwidth requirements or by sharing communications circuits using techniques such as simple time division multiplexing and packet switching; digital signals can often be communicated more accurately since error detection and error correction codes can be used, and because wide dynamic ranges can be handled; digital signals provide flexibility because they permit a tradeoff between distortion and noise immunity; and digital bitstreams can be encrypted to provide security.

Digital Voice

Two basic techniques for digitizing voice signals are waveform coding and source coding. With waveform based methods, the reconstructed analog signal *looks* like the original input signal, whereas with source coding the reconstructed signal is intended to *sound* like the original even though the waveform itself may look quite different.[1] Waveform techniques are simpler than source coding techniques but they require more bandwidth for the transmitted signal.

The quality of the regenerated speech is determined by its intelligibility, an objective but not yet automated criterion which measures how well the speech can be understood, and by its naturalness, a subjective criterion that indicates the listener's ability to recognize the speaker and to gain emotional and other cues from the speech. Although there are many digitization techniques, quality depends primarily upon bit rate. Three rough ranges of bit rates can be used to categorize digital speech: above about 12k bits/s, where the speech is often termed "toll quality" and is comparable to analog telephone speech; between about 6k and 12k bits/s ("communications" quality), in which the speech is highly intelligible but suffers noticeable degradations, such as distortion; and below about 6k bits/s ("synthetic" quality) in which there is a significant loss of quality.[2]

Straightforward pulse code modulation (PCM) is the most widely used digitization method, in which the analog waveform is sampled (after being low pass filtered) at 8 kHz and the amplitude of each sample is encoded in 8 bits, yielding a data rate of 64k bits/s. The quality obtained with PCM is quite high, standards exist for this method, and large scale integration (LSI) codecs implementing these standards are now available at relatively low cost. The disadvantage of PCM is that

Ed Note: Material in this column is derived from a communications technology forecast[3] the author recently carried out for the National Library of Medicine.

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For more information on products or employment opportunities, call or write today: Centronics Data Computer Corporation, Hudson, New Hampshire 03051, (603) 883-0111.

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CIRCLE 9 ON INQUIRY CARD

the analog bandwidth required to transmit the digitized signal is significantly greater than that required for the original analog speech waveform. A major use of PCM is in digital telephone switching equipment in which the analog voice signal is digitized, routed through the switch in digital form, and then converted back to analog for transmission. PCM is also used over digital links when high quality speech is required, especially if security is essential.

In order to achieve lower bit rates, simple waveform encoders based on delta modulation can be used down to about 24k bits/s. With this technique, a single bit is used to represent the difference between the current and previous samples of the analog waveform. Highly intelligible though somewhat noisy speech can currently be obtained with delta modulation, and implementation can be realized with a few LSI devices. In order to compensate for the degradation introduced by the 1-bit quantization used in delta modulation, the signal must be oversampled, ie, sampled at a rate higher than the minimum or Nyquist rate, which is twice the highest frequency component, approximately 8 kHz for voice. Differential PCM, which samples the waveform at the Nyquist rate but which uses more than 1 bit/sample, is effective at lower rates; and adaptive differential PCM, which uses a variable quantization size, can be used at even lower bit rates, currently down to about 16k bits/s, although the output speech at this rate does not quite achieve toll quality.[3,4]. As data rates are lowered further, the quality provided by all these techniques deteriorates rapidly.

Below about 12k bits/s the digitization technique must take advantage of some of the redundancy in the speech waveform; specifically, waveform encoders must use a changing rather than a fixed predictor. Hence the methods become more complex and more expensive to implement. In the rough range between 6k and 12k bits/s, adaptive predictive coding provides reasonable quality. With this technique, the transmitted signal comprises parameters which characterize the speech waveform together with a 1-bit error signal representing the difference between the actual input speech and the estimate derived from the model. At the receiver, speech is regenerated by applying the error signal to a filter derived from the parameters of the model. Present day adaptive predictive coders are relatively expensive because of their complexity, but they can achieve reasonable quality, and in fact, toll quality speech has been realized at 16k bits/s.

Below about 6k bits/s encoding devices must use a model of the speech waveform, and are hence called speech source encoders. The model consists of a binary voiced/unvoiced source exciting a time-varying filter (or filters) representing the short term spectral envelope of the speech signal. An error in the voiced/unvoiced decision can easily be heard as a distortion of the output speech, and therefore accuracy of the input waveform is important. The main difference among the different types of voice coders (vocoders) used is in the representation of the spectral envelope. Two techniques are channel vocoding and linear predictive vocoding (LPC). Channel vocoding, the older technique, is based upon spectral analysis and uses a bank of bandpass filters to obtain estimates of the speech parameters in each frequency subchannel. LPC makes use of an all-pole model of the speech spectrum (a frequency domain representation). The lowest data rate at which reasonable quality can be obtained with these techniques is about 2.4k bits/s; lower rates might be satisfactory for particular speech waveforms (eg, for certain speakers) but cannot be used generally because the vocoder must often be carefully tuned to the speaker. Because they operate at lower data rates, these analysis/synthesis techniques must make accurate estimates of the speech parameters in order to allow the signal to be adequately regenerated. These estimates cannot be made reliably on a degraded signal, for example, one that is noisy or one that has passed through the microphone in a standard telephone handset.

In the next few years there should be progress in terms of both cost and quality in each of the three ranges of bit rates. At the higher data rates, the quality of adaptive predictive PCM devices should improve by the early 1980s, and some cost improvements may result by the application of charge coupled devices (CCDs). At 16k bits/s, the quality of these units is good enough that a decision on their installation can be made on strictly economic grounds, and as implementation costs decrease by the mid-1980s, these devices should be increasingly utilized because of the 4-fold reduction in data rate they provide over PCM. In general, both PCM and adaptive predictive PCM should find increasing application over short haul and local circuits where the cost of the terminal equipment dominates, that is, where bandwidth is less critical. At the lower data rates, below 6k bits/s, speech quality will probably not improve substantially over that available today.

The major technical and economic impacts in digital voice communications will likely occur in the 6k- to 10k-bit/s range due to strong Department of Defense interest in devices in this range, and because the technology is amenable to microprocessor implementations. Good quality devices at 9.6k bits/s should be available in the early 1980s with costs initially in the several thousand dollar range, but substantial price reductions will occur as the market for the devices increases. These devices should be robust in a communications sense, in that they will be able to tolerate background noise, channel errors, or degradation that might be introduced by conventional telephone handsets and the associated wiring between the handsets and the telephone switch. The main attraction of the 9.6k-bit/s rate is that it is compatible with modems used with ordinary terrestrial phone lines. In this connection it is important to note that the error performance of these lines degrades the speech quality of current 9.6k-bit/s devices so that the output speech is not quite acceptable; however, even a relatively small improvement in the encoding technique can make a significant difference in the communications performance that is obtained. In other words, a major breakthrough is not required for these devices to gain a wide market.

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Part 2 of Dr Richer's column, to appear in the August issue, will discuss image digitization.

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CIRCLE 10 ON INQUIRY CARD

The HP 2621: sim

Simple doesn't have to mean unsophisticated. The proof is in our new CRT terminal, the HP 2621.

Before building it, we took a long, hard look at the way you use a simple terminal. Then we took the knowledge gained in more than 10 years designing computer products and applied it to engineering an interactive character-mode CRT terminal from the user's point of view.

The outcome was actually two models. The HP 2621A, which sells for $1450. And the HP 2621P, which has a built-in printer, costs $2550. You obviously want the sharpest display made. So we used the 9x15 character cell you see on every HP CRT terminal, including the top-of-the-line. And, to help you look back at the data you've entered, we provided two full pages of continuously scrolling memory.

We designed the keyboard like the familiar typewriter, so you don't have to waste time relearning it. We built in eight function keys, too. These control the cursor, rolling and scrolling. And, to make life easier, they're labeled on the screen for self-test, configuration, display and editing.

Editing? On a simple terminal? Certainly. We included character and line insert and delete, clear line and clear display. And, since the 2621 keeps your input separate from your CPU's, you can edit data before sending it to the computer. All without writing a line of system software.

Since flexibility is important in interfacing, we included a user-definable return key that will send your computer whatever code it expects. We also made our terminals compatible with RS232C and Bell 103A, and able to communicate with your CPU at 110 to 9600 baud.

If you need hard copy at your fingertips, take a look at the HP 2621P. With a keystroke, its built-in 120 cps thermal printer will deliver a printout from the screen in seconds.

So why don't you check out the HP 2621 by calling the nearest HP sales office listed in the White Pages. Or send us the coupon. Then see for yourself how sophisticated a simple CRT terminal can be.

Try this on your favorite CRT! With the 2621P, you just hit a key and in seconds you have hard copy of your CRT display. The built-in thermal printer prints upper and lower case at up to 120 cps.

The 2621's bright, high-resolution CRT, with enhanced 9x15 character cell, displays the full 128-character ASCII character set, including upper and lower case, control codes, and character-by-character underline, in 24 80-character lines.

Eight screen-labeled preprogrammed function keys magnify the power of the 2621's keyboard. Preprogrammed functions include editing, terminal configuration, printer control and self-test.

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CIRCLE 11 ON INQUIRY CARD

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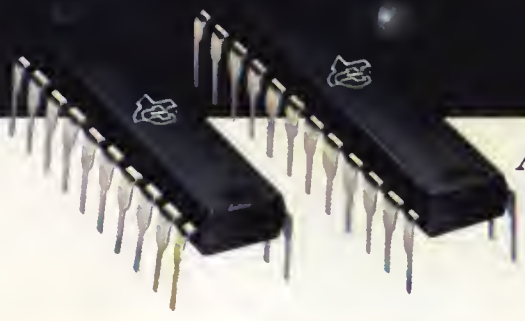

An advance look at third generation TTL.
Highest speed. Lowest power. Ever.

Two new Schottky TTL families. An alternative to ECL. New dimensions in low-power logic. From Texas Instruments.

Until now, when you increased processing throughput rate, you paid a power penalty.

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Now Texas Instruments offers you the most sought-after features on both ends of the bipolar speed/power spectrum... a whole new generation of advanced families of Schottky TTL.

A generation that will spawn new and significant improvements in efficiency, density and power-budgeting options.

So, if you need exceptional speed, you now have a way to increase both the complexity and performance of your MSI and SSI functions.

And you also have an advanced low-power Schottky TTL family that's 2.5 times faster than today's popular 74LS family, at half the power.

Just examine the features, functions and benefits of our two new advanced Schottky TTL families and we're sure you'll agree.

It's the best thing that's happened to bipolar logic since TI made TTL the industry standard more than 14 years ago.

New 24-pin package

New 300-mil wide, 24-pin ceramic and plastic DIPs, in which many MSI functions will be offered, will allow the designer to virtually double the functional densities while reducing board space by 30% or more. This increased density, coupled with an increasing breadth of product selection, will provide significant improvements in efficiency and reliability—reliability in keeping with TI's proven track record of high quality standards for semiconductors.

Advanced Schottky

Featuring a typical 1.5-ns gate delay and a 20-mW gate power dissipation, the new Advanced Schottky (AS) Series is twice as fast as any Schottky device available before.

PROJECTED SAMPLE AVAILABILITY

Advanced Schottky

Part Number	Description	Available
SN54/74AS804, 05, 08, 32	Hex 2-Input Gates	2Q79
SN54/74AS857	Universal MUX	4Q79
SN54/74AS881	4-Bit ALU	4Q79
SN54/74AS882	ALU Look-Ahead	4Q79
SN54/74AS873	Octal Latch	4Q79
SN54/74AS874	Octal D Flip-Flop	4Q79
SN54/74AS894	Shifter/Scaler	1Q80
SN54/74AS870	Dual 48x16W File	1Q80

Advanced Low-Power Schottky

Part Number	Description	Available
SN54/74ALS74	Dual D Flip-Flops	2Q79
SN54/74ALS109, 112, 113, 114	Dual J-K Flip-Flops	3Q79
SN54/74ALS00, 01, 02, 03, 04, 05, 08, 09, 10, 11, 12, 15, 20, 21, 22, 27, 30, 32, 133, 260	Gates	4Q79
SN54/74ALS28, 33, 37, 38, 40	Buffer Gates	4Q79
SN54/74ALS373, 573, 873	Octal Latches	1Q80
SN54/74ALS374, 574, 874	Octal D Flip-Flops	1Q80

Internal gate delay for MSI functions is typically 1 ns, while power consumption is only 12 mW.

The AS Series, a combination of new high-performance 20 and 24-pin functions designed specifically for high-speed applications, will encompass the MSI arithmetic operators and supporting gate and flip-flop functions required to implement high-speed CPUs, controllers, processors, and more.

Advanced Low-Power Schottky

Featuring a typical 4-ns gate delay and 1-mW gate power dissipation, the new Advanced Low-Power Schottky (ALS) Series will consist initially of 75 popular device types currently in the LS Series, including gates, dual D and J-K flip-flops, and MSI functions.

In addition, the new ALS Series, with the same drive as today's popular LS Series, allows immediate plug-in to existing logic systems.

The ALS Series, offered initially in familar socket-compatible packages, will ultimately encompass more complex MSI products in the new 300-mil wide 24-pin DIPs.

Fully compatible

Both the new AS and ALS Series will be fully compatible with the 54/74, 54/74LS and 54/74S TTL Series, in both military and commercial temperature ranges.

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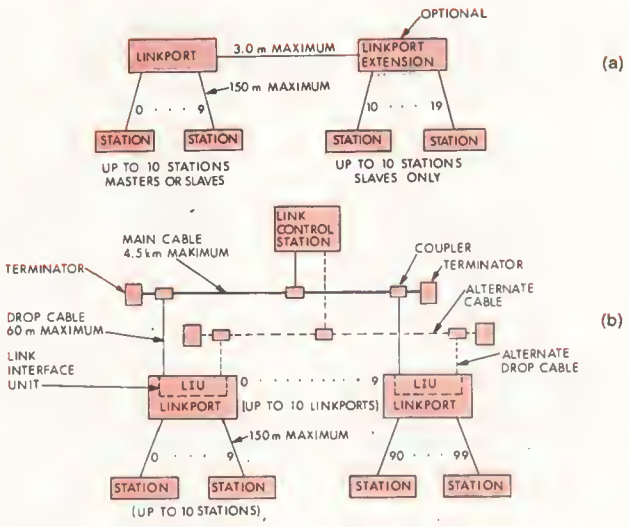


Cluster network (a) and linked cluster network (b). Former is basic building block of latter configuration, which links multiple clusters (equipment centers) in different plant areas into common communications subsystem. Dashed lines indicate backup or redundancy options

A microprocessor based series of systems for process management and control, designated Spectrum, was recently introduced by The Foxboro Co, Foxboro, MA 02035. Spectrum offers various standard configurations that provide the hardware and software integration for desired levels of process management, control functions, and process/operator interface.

Key element in the series is Foxnet, a high speed process communication subsystem which links processors and other electronic control equipment within discrete process management and control systems into an integrated network. With this link, control functions can be distributed throughout the plant, and stations such as processors, controllers, process I/O, and operator display consoles can communicate with one another.

Foxnet is composed of linkports (LPS), the transmission medium, and link control stations (LCSS) which function as the arbitrator for master stations seeking control of the communications link. There are two network architectures, cluster, (basic building block of the system), and linked cluster. The first comprises one or two LPS and up to 20 stations, and is used when stations are centralized within a 150-m radius. A linked cluster is required when more than 20 stations are needed, or when the LP and its stations are separated by more than 150 m. Linked cluster configuration adds the transmission medium, link interface unit (LIU), and LCS to form a user-configured network, and may contain as many as 10 LPS and up to 100 stations.

Long range transmission to a maximum of 4.5 km is by an industrial grade semirigid 75-Ω coaxial cable. Transmission rate is 1M bits/s. Communications protocol is based on a message framing format similar to SDLC and is transparent to the user.

CRT consoles provide for operator interaction, and display current process and network status, and live plant data. Standard or user-written software allow direct operator intervention based on data received from individual loops, trending information, or process alarms.

Circle 400 on Inquiry Card

Packet Network Offers Offpeak rates

A tariff for an offpeak rate for high volume nighttime and weekend usage has been filed with the FCC by Telenet Communications Corp, 8330 Old Courthouse Rd, Vienna, VA 22180.

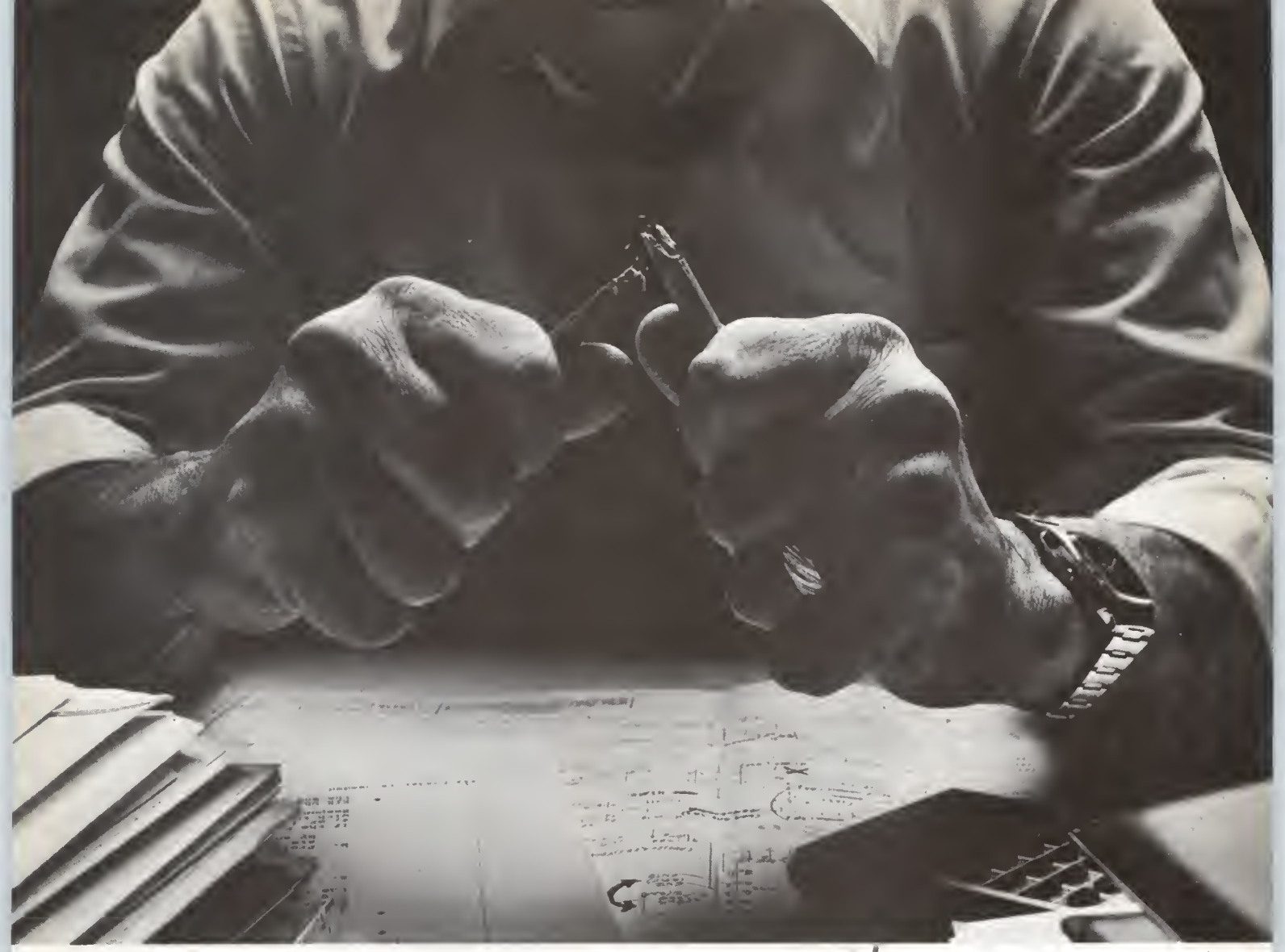
The service, called Nightline, is aimed at the home and student market and such potential users as college and university computing centers, and computer service bureaus whose offpeak usage exceeds several thousand hours a month. Organizations will be able to provide access to their computer centers from 180 U.S. cities for $0.75/h, which charge includes network connection time plus up to 2k packets of traffic per hour. Minimum charge for each subscriber organization is $7500/month.

The new rate applies between 6 pm and 7 am local time on weekdays, all day Saturday and Sunday, and on New Year's Day, July 4, Labor Day, Thanksgiving, and Christmas.

Report Reviews Advanced Signaling Concepts

National Telecommunications and Information Administration (NTIA) Report 79-13 discusses the design of the control signalling system for future all-digital communication systems. The report, "Control Signaling in a Military Switching Environment," reviews advanced signaling concepts available today, networks in general, and the military switching environment in particular. Network control functions are defined, and ways and means of performing these functions are described. The publication also makes recommendations as to the choice of signaling schemes. An 87-item reference section provides useful bibliographical data, and 54 figures and 40 tables complement the text.

The report was prepared by R. F. Linfield of NTIA's Institute for Telecommunications Sciences for systems designers and engineers involved in planning and operation of advanced communications systems. It is available from the National Technical Information Service, 5285 Port Royal Rd, Springfield, VA 22161. Accession No is PB 292-377/AS. Price is $9.25.



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Options available with the 415 Data Processor include an I/O board, 32K words of add-on memory, real time clock, two asynchronous ports, a parallel printer port, a synchronous port, front panel, and 4 or 8 port multiplexers.

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XPRT X.25 protocol tester is a multipurpose design, test, and training tool for developers and users of X.25 software and hardware. X.25 has been approved by the International Consultative Committee for Telegraphy and Telephony (CCITT) as a protocol standard for interfaces between data terminal equipment (DTE) and data communications equipment (DCE) operating in the packet mode.

The device tests, debugs, simulates and monitors X.25 equipment at each of the three defined X.25 levels (electrical, link, and packet) by generating, displaying, and validating X.25 traffic. The standalone unit is a complete hardware and software package supporting multiple line speeds, and requires no additional programming. Full documentation is provided.

The tester, under user interactive control, simulates DTE or DCE, monitors X.25 lines, generates and displays frames and packets in both directions in a legible format, monitors and reports error conditions, and provides loopback testing.

Direct connection to the device under test is via v.24/RS-232-C. Remote connection is through modems over a 600-bit/s synchronous full duplex line. Interactive control is by means of teletypewriter or video console through standard v.24/RS-232-C interface, using ASCII code at standard speeds to 9600 bits/s. Console display is command selectable in either hex or octal notation.

Developed by Tran Telecommunications Corp, 2500 Walnut Ave, Marina del Rey, CA 90291, the tester is packaged in an 8.9 x 48.3 x 50.8-cm housing. An optional logic specification document providing flow chart level details of X.25 implementation is available. Deliveries are scheduled for Sept 1979.

Circle 401 on Inquiry Card

Software Package Links DEC Datasystems, Mainframes

Designed for data-intensive EDP applications, RDCP 2780/3780 is a batch-oriented communications software package that permits DEC Datasystems to communicate with one another and IBM mainframes using both 2780 and 3780 protocols. The package, for use with Datasystem 150, 320, and 350 configurations, is available from Digital Equipment Corp, Maynard, MA 01754.

Features permit users to perform semiautonomous operations at the Datasystem level while at the same time allowing central data processing personnel the control required to supervise the network from a central location. Data can be transferred on a batch basis concurrently with other Datasystem operations; both data and software can be transferred. Memory requirements for the package are 56k bytes min.

Circle 402 on Inquiry Card

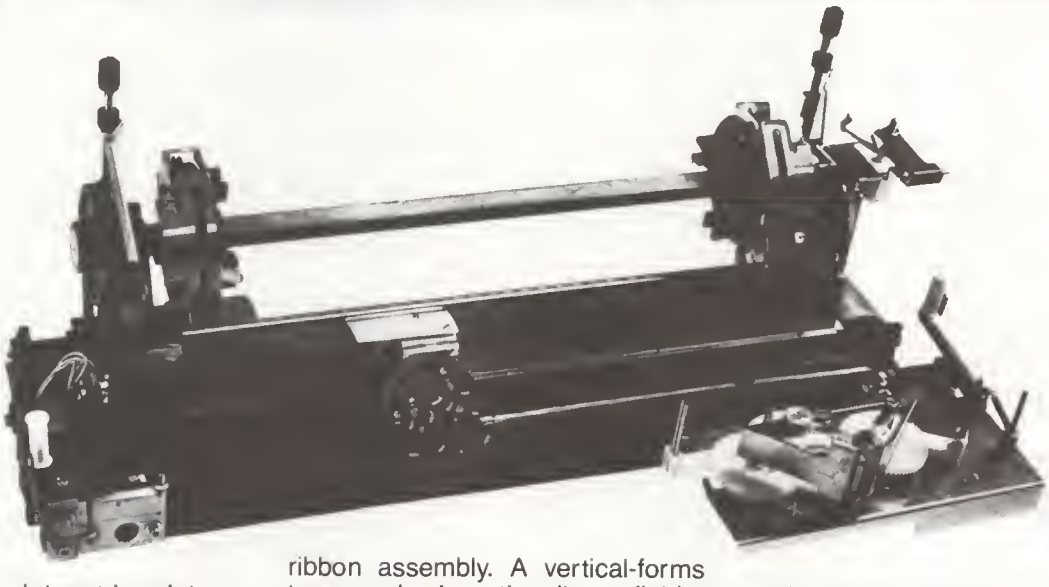
U. S. Cities and International Nodes Added to Packet Net

The addition of 14 more local-call-access U.S. cities to its domestic network has been announced by Tymnet, Inc, 20665 Valley Green Dr, Cupertino, CA 95014, operator of TYMNET public packet communications network. This brings the total of cities serviced by the network to 165.

The cities added are Burlingame, Marina del Rey, and San Pedro, Calif; Union and South Brunswick, NJ; Springfield, Mass; Winston-Salem, NC; Evansville, Ind; Albuquerque, NM; Greenville, SC; Richland, Wash; Charleston, W.Va; Peoria, Ill; and Hempstead, NY.

International access was also established from Sydney, Australia and Tokyo, Japan through agreements with International Record Carriers (IRCS) and overseas Post, Telephone and Telegraph (PTT) administrations. □

The race for dot-matrix printer sales can be won by a head!



If you're selling dot-matrix printers, chances are you'll win — or lose — by a head. The speed, reliability and versatility of the print-head mechanism can make or break your product.

Florida Data's PB-600M/BNY-M is a heavy-duty matrix printer mechanism designed for high print-volume applications.

Selecting the PB-600M or BNY-M will assure you, as the OEM, of highest performance and maximum value added. FDC supports these products with complete documentation, including all analog and logic circuits, power supply recommendations and packaging. This support enables the OEM, at minimum development expense, to produce a complete, high-performance printer.

The mechanism includes a print-head, rail assembly, timing disc assembly, motors, paper tractor and ribbon assembly. A vertical-forms tape reader is optionally available. The BNY-M uses a high-speed stepper motor and a dual-track timing disk for high resolution characters and 128 dot/" graphics.

The print-head employs magnetic stored-energy wire hammers — a technology developed by FDC. The eight-wire head is capable of hammer rates as high as 3,000 cycles per second, with no duty cycle or page density restrictions. This translates to 600 characters per second for 8 x 7 matrix printing, or 240 lines per minute for 132 character/line format. For shorter lines, the unit is capable of over 1,000 lines per minute.

FDC's PB-600M/BNY-M prints an original plus seven copies and handles forms from 2" to 15" wide. Paper slew is 8"/sec. for the PB-600M and 13"/sec. for the BNY-M. Either unit weighs approximately 20 lbs. and is 21½" wide x 9" high x 12."

The mechanism is bi-directional, fast and almost unbelievably durable. It lets you offer your customers line printer speed with serial printer economy, and it's been field-proved in our own PB-600 printers.

Before you invest another dollar in printer development, find out what Florida Data can do for you. Write for further technical data or call 305/724-6080 to arrange a demonstration.

Florida Data Corporation
3308 New Haven Avenue
West Melbourne, FL 32901

FDC

Created by Hall & McKenzie, Inc., Winter Park, Florida

CIRCLE 16 ON INQUIRY CARD

F6800 SERIES

We've just added two hard-hitting rookies to our winning lineup.

Now that the new F6802 microprocessor and F6846 combo chip have joined Fairchild's F6800 team, you've got a minimum, microprocessor-based-system solution to your design problems. One that's low cost and easy to work with too. Like the rest of our F6800 family, these two great new NMOS products are made using Fairchild's patented Isoplanar™ process.

The F6802 and F6846 are already becoming big hits in the microcomputer field. When you put them on your team, they're bound to score some winning runs for you.

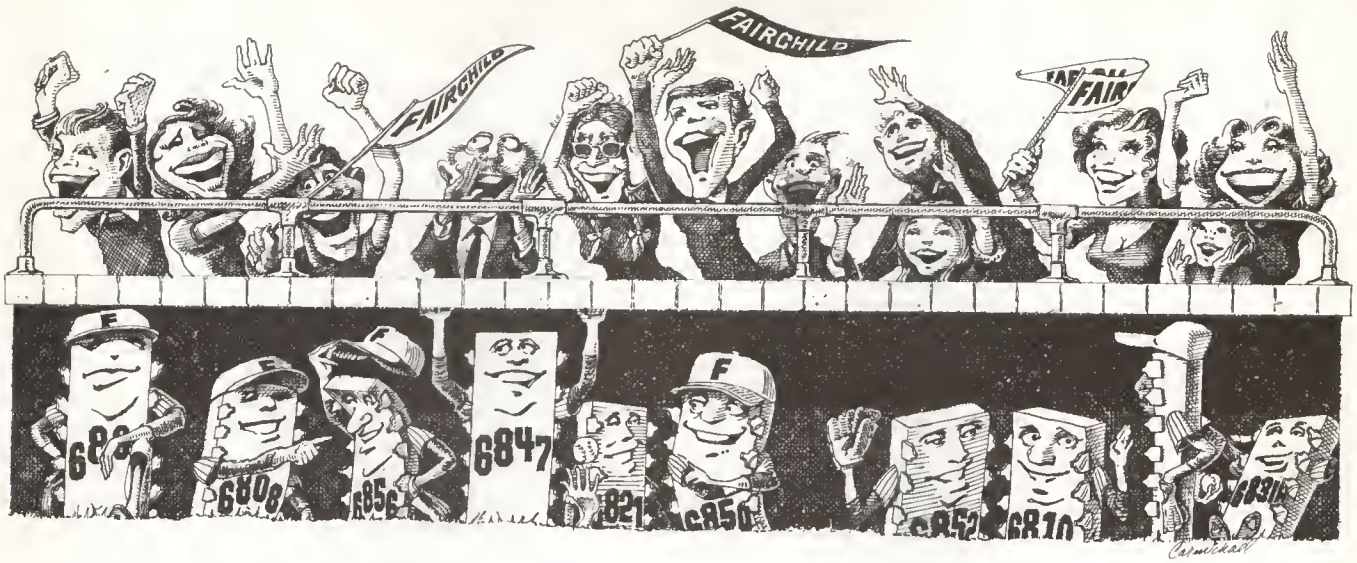
The F6802 microprocessor. It sends your design problems to the minors.

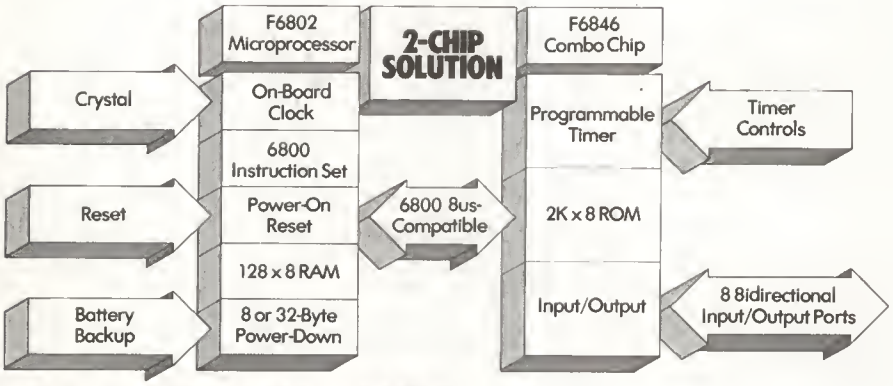
And that's where they'll stay, thanks to this enhanced version of the F6800 central processing unit. The F6802 offers an on-chip power-on reset function, on-board clock for easier use and on-board 128 x 8 RAM with options of 8-byte or 32-byte power-down. Now you no longer need an additional RAM with battery backup systems.

The F6802 features a memory-ready line for slow or fast memory. So you can use memories in synchronous or asynchronous mode. And the F6802 is bus-compatible for easy use with all of the other F6800 peripherals.

The F6846 combo chip. It's a memorable teammate.

The F6846 is a user-defined ROM-based peripheral element. It features 2K x 8 ROM, a powerful programmable binary timer, and eight bidirectional input/output ports on the same circuit. It's also F6800 series bus-compatible.





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No matter what your needs, from standard to hi-rel, we can supply you because our F6800s are in stock at our distributors now. In quantity too, so you can have on-time delivery.

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TECHNOLOGY AND ECONOMICS: POTENTIAL COMPUTER MARKET ELASTICITY—I

Montgomery Phister, Jr

Systems Consulting
Santa Monica, California

Since the beginning of the computer era, the marketplace has absorbed equipment almost as fast as manufacturers produced it. However, those in the industry must be aware of the possible limitations on that market. The potential elasticity of this market derives from various factors that influence the demand for data processing systems. Examination of first the number of organizational units which have data to process, and second the amount of processing that these units have to do provides some insight into the ultimate market. A second column, to be published in August, will speculate on what activities can be expected in a saturated market and will conjecture that there is a limit to the amount of processing to be done, and therefore ultimately to the amount of equipment that can be sold.

Limiting Factors

At any given time, a user's data processing (DP) requirements can be described by a curve like the dotted line in Fig 1, and a computer system's price/performance characteristics by a curve similar to the solid lines in the figure. Of the three computer systems shown, only system C1 meets the given user's requirements economically. System C3 configurations generally do not have enough power to solve the problems or are too expensive, if they do have the required power. While system C2 has adequate power, it is too expensive.

If, as in Fig 2, a point placed near the inflection point replaces each user and system curve, it should be apparent that a given computer can profitably serve any user that appears above and to the left of it on the graph. Thus system C1 can serve both users U1 and

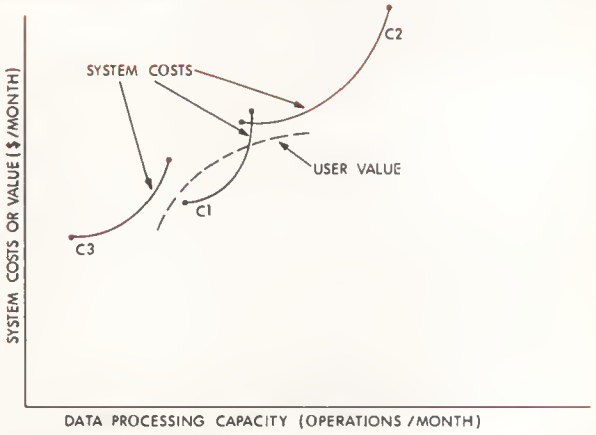

Fig 1 System costs and user value. Dotted line shows amount specific user is willing to pay for given amount of processing capacity. User implements most rewarding applications first; if offered more and more capacity, he finds less and less profitable uses for it, and thus is willing to pay less and less for each increment. Solid lines describe price/performance characteristics of three different computer systems. Each system provides minimal level of performance at minimum price, as indicated by lower left end of each solid line. As memory, peripherals, and auxiliary processors are added, price and performance increase. First price increases give large performance improvements, but later improvements are more expensive, and each system has maximum size and capacity

Introducing the NEC Winchesters.

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You've heard about NEC's fine printers. Now let us tell you about NEC's fine family of Winchester-type disk drives. The D-1200 series

There are three models—with 20, 40 and 80-megabyte capacities. Each has an industry-standard storage module device (SMD) interface that makes it immediately attachable to any mainframe or minicomputer that uses storage module disks.

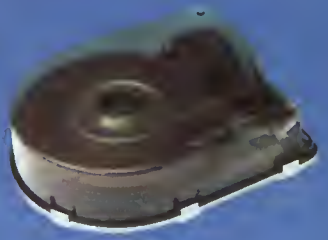
But that's just the beginning.

The NEC D-1200 Series is fast. Latency time of 8.3 milliseconds. Data transfer rate of 1.2 megabytes/second.

The NEC D-1200 is reliable. Its 10,000-hour MTBF is made possible by the encapsulated fixed disk and contact fixed read/write heads. Each head has its own LSI preamplifier which reduces errors by improving signal-to-noise ratio.

The NEC D-1200 is flexible. It has a dual-port option so two CPUs can share a single disk. Its address mark detector option saves system time in seek-and-search operations. Its two head-per-track options eliminate seek time and speed up overall performance. There's a front panel option with ready, fault, write/protect and off-on features.

The D-1200 is all-NEC. Circuitry, power supplies, the sealed Winchester module with its recording media, read/write heads, LSI circuits and rotary actuator are designed and built by NEC—the company with 15 years experience in developing and manufacturing disks.



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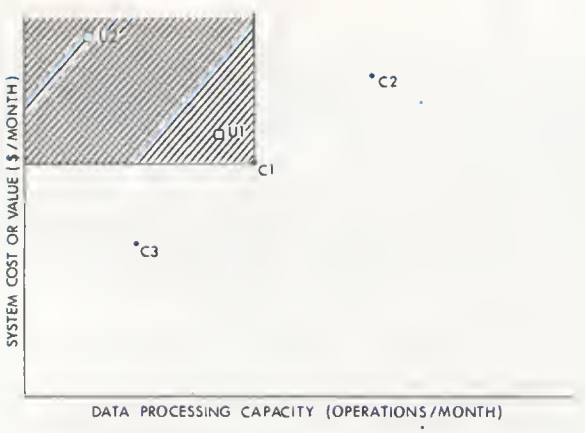

Fig 2 Matching system to user requirements. With each user and computer system represented by point, note that computer can profitably serve any user appearing above it and to its left on the graph. Computer C1, for example, has sufficient power to serve any user in shaded area, and costs less than value of all user applications in that area. Note that systems C2 and C3 cannot economically serve user U1, but can serve U2

U2, along with any other user whose requirements lie in the shaded area. Note that user U2 could profitably use any of systems C1, C2, or C3, though of course C3 would yield the best return on his investment.

At any given time, there are a finite number of locations in the U.S. where data are processed. These sites exist within companies, government agencies, associations, homes, etc, and each can be plotted as a user point on a value/capacity graph. Fig 3 is an attempt to plot all U.S. users' points, and to count the number of points in various value/capacity ranges. The notation in the lower left square, for example, estimates that there are approximately 10 million locations that require a data processing capacity of up to 10 operations/s, and could afford to pay up to $10/mo for that capacity.

In the early days of the industry, computer power was expensive, and relatively few users could justify the cost of the available systems. The shaded area in Fig 4, for example, estimates the number of potential users of the computers available in 1954 (see Ref 1, pp 160-166). With every passing year, however, technology has made it possible to provide computer power at lower and lower costs, and today the technology limits are approximately as shown by the dotted lines in Fig 4. The lowest cost minicomputers, small business computers, and word processing systems are available at the equivalent of less than $100/mo, and the most powerful general purpose computer systems provide equivalent capacities of over 10 million operations/s. In the years to come, the dotted lines should continue to move down and to the right.

International Data Corp has for some years kept track of the growth of the computer industry, and has defined three categories of computers, called "general purpose" (GP) systems, "minisystems," and "small business computers" (SBCs).[2] The GP market grew more or less exponentially during the 50s and early 60s, but has recently leveled off. The minicomputer market started in the mid-60s and still seems to be in a near-exponential growth phase. The SBC (and word-processing system) markets have just been getting started in the mid-to-late 70s. Fig 5 shows the growth of these

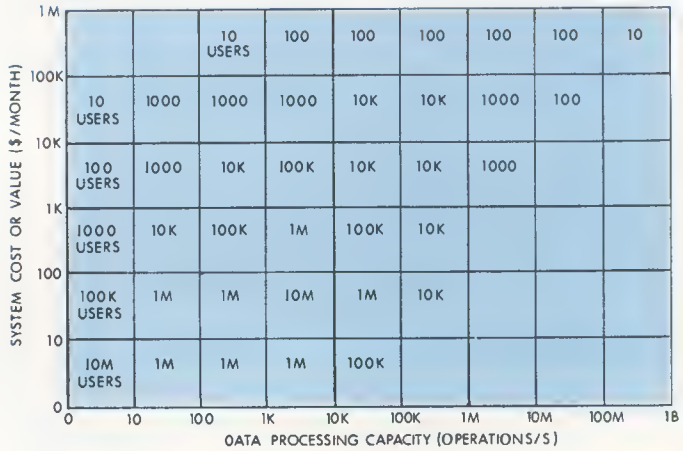

Fig 3 Potential users vs system value/capacity ranges. If each potential U.S. DP user is plotted as point on value/capacity graph, result is an estimate of number of points (and thus number of potential customers) in each value/capacity range. Numbers in squares are author's estimate, to nearest power of 10, of how many locations in U.S. could use DP capacity in range indicated by abscissas, and could afford to pay amount indicated by ordinates of square

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Computer maintainability has always been one of the biggest headaches for the OEM – not to mention the end user.

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But the SCOUT NAKED MINI 4/04 solves that problem with its unique new ISOLITE self-test feature.

When SCOUT is turned on – or when your program commands it – the ISOLITE circuit automatically checks the status of each logic board. As each board is tested, a small LED (Light Emitting Diode) attached to the board's edge comes on. In a few seconds, if the board passes, its LED goes out. If the board fails, its LED remains on to indicate a failure – which makes it easy for an OEM or end user to quickly find and replace the faulty board.

The user can add test programs for his own special devices attached to our I/O controller. And since every function is totally contained on a separate board, it is easy to isolate failures.

Serviceability, in short, is unequalled. And it's not only a tremendous maintenance advantage for the OEM, but it's a truly unique advantage for the end user.

IT'S NOT HOW SMALL YOU MAKE IT. IT'S HOW YOU MAKE IT SMALL.

Usually, when the package gets smaller, so does the performance. For the OEM with big ideas and no place to put them, this means making a compromise on computer capability.

But all small packages are not equal, as the SCOUT NAKED MINI 4/04 demonstrates.

The form factor, to be sure, is rather remarkable. All boards are a mere 6.25" x 8.3".

But still more remarkable is the extraordinary performance produced by a machine this size.

The SCOUT NAKED MINI 4/04 CPU archi-

tecture is fully compatible with other NAKED MINI 4 family members. SCOUT provides multiply/divide instructions, a real-time clock, power-fail and auto-restart as standard features. Floating point instructions are available as an optional feature.

What's more, SCOUT is word or byte addressable—with direct addressing of 128K bytes—and fully supports multiple DMA and interrupt devices.

SCOUT's supporting system and function boards add up to make SCOUT a versatile performer.

Your choices include: A RAM memory with up to 128K bytes. A RAM/EPROM memory. A remote console. A 16-channel analog-to-digital converter. An 8-channel relay output module. A parallel 16-bit I/O controller. A serial I/O controller. An extender card (to permit system expansion). Plus a prototype module and, last but not least, two +5V power supplies and card cages.

Obviously, a minicomputer that gives you the flexibility to configure so many ways is a lot more than just a hot-shot new computer. It's a computer system.

Predictably so, because ComputerAutomation has always been the place the pros go for systems-oriented minicomputers.

So from the word go, SCOUT gives you everything you need to succeed. In terms of size. In terms of 16-bit computer power. And because it's a complete system.

SO MUCH SOFTWARE, SO SOON?

Sure. Because SCOUT is a compatible member of the NAKED MINI 4 family.

For openers, there's our Real-Time Executive (RTX). It's precisely what you need for building your own real-time applications.

Also, SCOUT will execute any Fortran IV program you've compiled on another NAKED MINI 4 development system.

Then there's our special INTRACOMM™ communications package to make computer-to-computer communication between NAKED MINI-based systems a snap. You can communicate data, or you can down-line load application programs to a remotely-located SCOUT.

For program development, there's OMEGA 4, our general-purpose, memory-based assembly language development system that runs on SCOUT.

Or, you get the flexibility to develop SCOUT software on any other NAKED MINI family computer. And that gives you access to our powerful OS4 software development system, multi-terminal editor, extensive utilities and high-level languages.

And that gives you everything you need to succeed—in terms of software.

HOW TO SCOUT YOUR PROFIT POTENTIAL.

Obviously you'd like your systems to be more competitive—and profitable.

So we suggest you do a little comparison shopping. Compare, for example, a typical SCOUT configuration consisting of, say, a CPU, 32K bytes of RAM memory, a parallel I/O and a 4-slot card cage.

What you'll discover is savings—maybe as high as 50%—over most other mini or micro solutions.

Because for just $985, our basic SCOUT is one tough system to beat when you get down to the ol' bottom line.

Of course, volume discounts further reduce your cost.

And that means, with SCOUT, you can trim your cost-of-product *and* beef-up your profit margins. All in one simple step.

Of course, you've got to consider the incomparables, too.

Because like every other Computer-Automation NAKED MINI computer, SCOUT is covered by the industry's only full-year warranty.

And, like no other mini, SCOUT provides a built-in ISOLITE self-test capability.

Even SCOUT's software is way ahead of the competition when it comes to putting the OEM first. To make it hassle-free, there are no licensing fees or per-copy charges to worry about.

Any way you look at it, SCOUT NAKED MINI 4/04 puts an end to the small talk.

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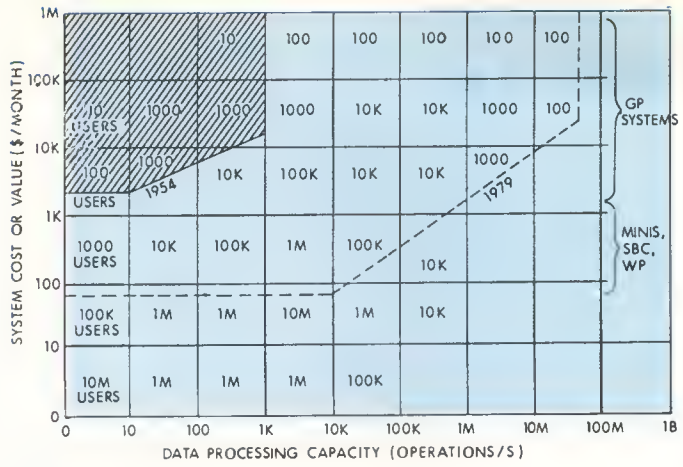


Fig 4 1954 vs 1979 market. In 1954, characteristics of available computers lay along diagonal line which borders shaded area. Of the few thousand potential customers whose requirements lay in that region, only about 100 had computers at year-end 1954. Today's potential market is enclosed by dotted lines. "GP system" portion of market is essentially saturated—virtually every potential location has computer system. Minicomputer, small business computer, and office automation markets are still far from saturated

markets, as measured by number of systems in use in the U.S.[1,2]

Saturated Markets

Saturation of the GP market, as seen in Fig 5, seems reasonable from the perspective of Fig 4: virtually all locations that can justify DP system costs above (about) $1500/mo have computers. Fig 4 requires the prediction that the minicomputer, SBC, and word processing markets will also saturate in the coming years, as potential locations for computers in process control, test equipment, data acquisition, business data processing, and office automation all acquire equipment. When will this saturation occur? The data of Fig 4 are not sufficiently precise to use in predicting a specific year, of course. However, with some 350,000 SBCs and minis in use at year-end 1978, and 1979 shipments expected to be over 150,000 systems, it is reasonable to expect to see 1 million units in use in the U.S. by year-end 1982—and I argue that 1 to 3 million systems will be near-saturation for the over-$100/mo (1978 dollars) business data processing applications. There will be further growth in word processing (or office automation) systems and in personal computing systems (at prices equivalent to $100/mo or less for the latter), but ultimately those markets, too, will saturate.

The term "saturate" as used in the previous paragraph describes the situation where every location that can use equipment has equipment, and the number of systems in use ceases to grow, or grows very slowly. Next month's column will consider the question: What activity can be expected in a saturated market? Putting the question another way, once a location has some DP equipment, what further equipment changes can be anticipated in the future?

References

1. M. Phister, *Data Processing Technology and Economics*, Santa Monica Publishing Co, Santa Monica, Calif, 1976
2. International Data Corp, *EDP Industry Report, Annual Review and Forecast*, (published each May), International Data Corporation, 214 Third Ave, Waltham, MA 02254

The author solicits comments on the material presented here, data supporting or contradicting his approach, and suggestions for topics to be explored in future articles.—**Ed.**

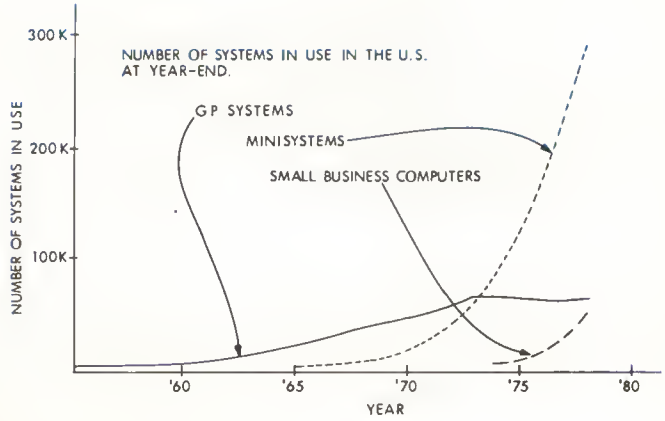


Fig 5 Number of systems in use. Estimate of number of systems in each classification in use in U.S. at year-end. "General purpose" systems are size of IBM's System/3 and larger, and are used primarily for business data processing. Minicomputer systems are used in process control, test equipment, and data acquisition. Small business computers are business data processing systems smaller than the System/3. General purpose market has been saturated since mid-70s, in sense that number of systems in use has stopped growing. (Word processing installations are not included in this graph)

8″ Rigid Disc System Offers 45M-Bytes In Floppy Size Package

An 8″ (200-mm) fixed disc system, the 1200 series from Micropolis Corp, 7959 Deering Ave, Canoga Park, CA 91304, provides 38% more storage capacity in 80% less space than existing 14″ (35.5-cm) drives. The units' 45M-byte potential capacity makes them viable candidates as primary mass storage devices in small mainframe, minicomputer, and microcomputer configurations.

System features include buffering for asynchronous transfers between host and controller, operation in direct mode for synchronous transfers at disc speed (approximately 1 μs/byte), and an error correction option to ensure data integrity. Designed using Winchester technology, the lower half of the drive package contains one, two, or three 200-mm hard discs, disc heads, voice coil motor components, and positioner, and is completely sealed. The upper half contains the electronics package on three circuit boards, one of which is the optional intelligent controller board. Components in the disc compartment are specified at 25k-hour MTBF.

Rotational drive for the discs is provided by a directly coupled brushless dc motor. This combination permits three plotters to be packaged in the 4.62″ (11.7-cm) high unit. Switching information for the electronic commutator is supplied by three phototransistor/LED combinations attached to the motor control PCBA.

Positioner is a swing arm mechanism supported on two preloaded bearings which reference to a stub shaft rigidly attached to the casting. Between two and four arms are accepted. The voice coil attaches to the system on the opposite side of the bearing from the head and the whole mechanism is statically balanced. Position reference is made to tracks recorded on a dedicated surface on the plotter nearest the deck.

Three boards are associated with the basic drive mechanism: preamplifier PCBA, motor control PCBA, and device electronics PCBA. Consisting of an 8 x 14″ (20 x 36-cm) board that resides in the drive assembly, the microprocessor based controller performs data formatting, encoding, decoding, sector buffering, error detection and recovery, and general housekeeping functions. Error correction is provided by an optional ECC board that attaches to the controller.

Measuring 8.55 x 4.625 x 14.25″ (21.7 x 11.7 x 36.2 cm), the unit fits within the outline of an 8″ flexible disc drive and requires the same supply voltages. Physical size permits full interchangeability, including matching screw mounting holes, with a typical floppy drive.

Vacuum sealed portion of Micropolis Corp's 8″ rigid disc drive as seen from bottom (through transparent enclosure for demonstration purposes). Available with 1, 3, or 5 recording surfaces, units offer up to 45M bytes of unformatted storage capacity in overall enclosure about 80% smaller than existing 14″ drives

The system interfaces to the host via an 8-bit bidirectional bus and nine control lines. The interface structure provides for programmed I/O and DMA data transfers. Data transfers of either a full sector or a full track may be made from one command. Special commands enable transfer of a full track in sector order. Maximum transfer rate is 929k bytes/s.

Three configurations offer 1, 3, or 5 recording surfaces on each drive and provide formatted capacities of 7.13, 21.4, and 35.6M bytes/drive using 1024-byte sectors. Standard recording formats are 72 sectors at 128 bytes, 42 sectors at 256 bytes, 40 sectors at 268 bytes, 36 at 320, 24 at 512 bytes, or 12 sectors of 1024 bytes. The unit uses the GCR encoding method and records 8750 bits/in (3444/cm) on the inner track; 580 tracks are available. Track to track access is 4 ms, with average access requiring 34 ms, and settling time of 8 ms. Reliability figures (excluding error correction) are given as 1 in 10^{10} soft read errors, 1 in 10^{12} hard read errors.

Representative of the price range is the mid-sized model 1202-1, with 27M-byte capacity at $1350 in 1000-unit quantities. The optional intelligent controller board is priced at $500 in OEM quantities. Quantity shipments are scheduled to begin in fourth quarter 1979.

Circle 175 on Inquiry Card

Winchester Type Disc Storage Systems Offer High Performance

High performance D-1200 series disc storage subsystems, using Winchester-type design, incorporate an industry standard storage module interface to facilitate attachment to mainframe or minicomputer. The 20M-, 40M-, and 80M-byte units from NEC Information Systems, Inc, 5 Militia Dr, Lexington, MA 02173 incorporate LSI circuitry to provide MTBF of 10k hours, and MTTR of 30 min.

Data reliability is enhanced by the use of a rotary actuator that assures rapid positioning of the read/write heads over each track. Each head has its own LSI preamplifier mounted near the head coil to improve the S/N ratio at the point closest to the recording surface. This reduces the risk of high noise levels that are a common cause of disc errors.

Major specifications of the units include start time of 30 ms and stop time of 20 ms. Latency is 8.3 ms, and average seek time is 40 ms. Recording code is MFM and interface code is NRZ.

Model 1210 is a single-platter, dual-head unit with one recording

Introducing the Tape Transport that thinks for itself.

Now, Datum innovation brings you the next generation in mini-computer magnetic tape transports, the D-451. A transport that thinks for itself thanks to Datum's smart new single-board microprocessor.

Self diagnostics, a reduced electronic component count and hybrid chip read amplifiers are examples of Datum's entirely new microprocessor design architecture.

You won't need an external test box with the D-451. Fault-isolation, and skew verify alignment are among internal microprocessor controlled self-test diagnostics.

An embedded Dual/Density formatter controls up to four tape transports.

Every aspect of the intelligent D-451's design and engineering makes its contribution in superior performance and reliability when reading and writing IBM/ANSI-compatible, ½" magnetic tape. Featured are: 7-or 9-track, NRZI and PE formats; dual format is standard for 9-track. Phase Encoded density is 1600 BPI, while densities of 800, 556 and 200 BPI are available for NRZI.

And Datum's painstaking research provides the D-451 with IBM tape-path geometry, ceramic blade tape cleaners, photoelectric write ring detection, low-inertia capstan drive and digital write deskew control.

Find out more about the reel thing, the tape transport that thinks for itself. Call or write your local Datum representative or Datum Inc., 1363 South State College Boulevard, Anaheim, California 92806. (714) 533-6333.

datum inc

CORPORATE HEADQUARTERS 1363 S. State College Blvd., Anaheim, CA 92806, Tel: 714/533-6333, TWX 910/592-1289, Telex 68-5579 • **EUROPEAN HEADQUARTERS**, DATUM (ELECTRONICS) LTD., DATUM House, Harlington, Middlesex, England, Tel: 01-897-0456, Telex 935-398 • **DATUM SALES OFFICES, CANADA**, Willowdale, Ontario, Tel. 416/491-6960, Telex: 06-966857 EOR TOR; **MOUNTAIN STATES**, Denver, Colorado 80232, Tel: 303/693-3414 **EAST COAST**, Mountainside, New Jersey 07092, Tel: 201/654-5590; **MIDWEST**, Des Plaines, Illinois 60018, Tel: 312/296-1064; **SAN JOSE**, San Jose, CA 95117, Tel: 408/249-5370; **NEW ENGLAND**, Framingham, MA 01701, Tel: 617/872-6911.

surface. The 1220 has two platters with four read/write heads and two recording surfaces. A 3-platter unit, the 1240 has eight read/write heads and four recording surfaces. Each also has an additional servo head associated with the drive's servo tracks.

Optional on all models is a fixed head mechanism that improves performance by eliminating seek time. A dual-port feature permits single or multiple clusters of drives to be accessed from two separate CPUs. An address mark detector option adds data security by insuring the validity of address mark information before transferring data to the controller. A front panel option provides operators with ready and fault indicators, a write protect switch, and an on/off switch.

Storage capacities are 20.8M, 41.5M, and 83.1M bytes unformatted for 1210, 1220, and 1240, respectively. Prices start at $2950, $3300, and $3870, respectively.

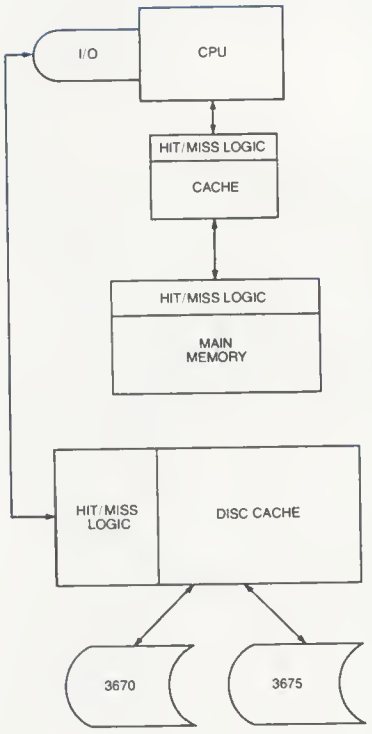
Circle 176 on Inquiry Card

Disc Cache Combines CCDs and Microprocessor For Fast Data Access

Combining CCD and microprocessor technology, the 3770 disc cache bridges the data access gap between the computer and disc storage devices. Developed by Memorex Corp, San Tomas at Central Expy, Santa Clara, CA 95052, the cache provides access to information in 2-ms rather than the 30 to 50 ms required when accessing directly from disc.

Designed for use with the company's 3670 (100M-byte) and 3675 (200M-byte) disc storage subsystems, the system can significantly reduce three primary components of disc data retrieval: seek time, rotational delay, and data transfer time. It is operationally transparent to all time-independent user programs and compatible with all IBM disc access methods and standard IBM operating systems. In tests the unit has been shown to improve run times by an average of 50%.

Use of CCDs for data storage offers the potential for approximately four times the storage density provided by RAMs at approximately the same cost. In addition the power dissipation per bit of storage for CCDs is far lower than that for any other major memory technology, simplifying the corresponding cooling requirement. These factors coupled with the relative speed of the devices can provide greater capability within existing disc systems, eliminating or deferring the need for costly conversions.



Memorex's 3770 disc cache increases performance of I/O bound mainframes by providing rapid CPU access to disc stored data. Using CCDs for dense mass storage, cache's microprocessor contains algorithm which maintains control of I/O requests

Since in most applications certain data elements are accessed more often than others, storing that data in cache provides significant increases in system throughput and performance. To assure that these data are in cache when needed, an algorithm in the system's microprocessor manages the memory area. All I/O requests are intercepted by the cache controller positioned at the head of a disc string. If requested data are not in the cache, the request passes through to the disc and the track containing those data is copied into cache. Highly active tracks can be retained in cache using the optional track lock feature to keep them readily accessible.

A standard model consists of the semiconductor storage unit, full track buffer, cache controller, flexible disc, power system, and operator control panel. Purchase price for a 1M-byte capacity system is $55,000.

Circle 177 on Inquiry Card

Semiconductor Disc Boosts Virtual Memory System Performance

FAST-3805, an IBM compatible semiconductor disc storage subsystem, emulates mechanical disc subsystems, but achieves faster access times and higher data transfer rates. Designed to enable IBM 370/303X virtual memory system users to attain better performance, the RAM based system from Intel Corp, Commercial Systems Div, 3157 N 34th Dr, Phoenix, AZ 85017 increases virtual page storage area, decreases virtual paging access times, and increases data transfer rates, thereby increasing system throughput and expanding processing speed capacity. In addition, the system reduces power requirements 60 to 80% and space requirements 50 to 80%, can be located 1.3 to 3.5 times further from the CPU, and adds data integrity by performing double-bit error correction.

Many IBM 370/303X virtual memory systems with 2305 fixed head discs and 3850 moving/fixed head discs have become I/O bound through heavy use of multiple virtual system (MVS), timesharing option (TSO), information management system (IMS), or high activity online applications. Even with adequate system speed this prevents users from adding users and performing more work. The FAST-3805, added to such a system, makes use of latent system capacity to avoid the need to upgrade or add a CPU,

WE FEEL LIKE A NEW COMPANY.

Maybe we should act our age.

But even though we're a dignified eleven years old, we can't help feeling vigorous and enthusiastic. Even cocky.

Century Data Systems was born in 1968 as a sharp little company making great big disk drives.

CalComp thought so, too. In 1974, we dropped our name in favor of theirs.

Since then we've gained the experience and maturity necessary to make us a leader in the mass storage industry.

Now it's the beginning of a new Century. We've gained Xerox as a parent. Our old name is back. And with it, a whole new spirit.

Spirited people and super new product families like *Marksman* and *Hunter.*

And the *Trident* family of proven, reliable, maintainable disk pack drives.

Plus the will and wherewithal to meet challenges head on.

To see what new and exciting things we have in store for you, just give us a call.

It'll make you feel like a new person.

Century Data Systems, 1270 N. Kraemer Blvd., Anaheim, CA 92806. Phone (714) 632-7111.

Century Data Systems
A Xerox Company

HUNTER LEAVES CO

The Hunter, featuring 16 MB removable and up to 80 MB fixed, is about to make a clean sweep in the cartridge disk feature race.

It employs a filtering system that removes particles down to .3 microns — proven in thousands of Tridents.

Unlike competition, it has a tunnel cover which keeps contaminants from reaching the pack area.

What's more, the Hunter reminds operators not to leave the cartridge bottom cover out to gather contaminants during operation.

And finally, the Hunter clean air seal isn't broken when the drive is serviced. (The competition's seal must be broken just to replace a fuse.)

Hunter wins hands up.

At this level of performance, you need a solid, rigid frame to help maintain accuracy and reliability. No tilts allowed.

And with Hunter, you get it.

Now, we wouldn't want to point the finger at anybody in particular, but some frames actually twist visibly when you lift one corner.

Try it.

Price fight.

We use an industry-standard 5440-type cartridge of proven reliability. It has no unusual features that could limit the number of media manufacturers or drive the price up. Like a servo surface. The competition, on the other hand, uses a unique cartridge that requires a written servo surface. Future availability and pricing could obviously be affected.

Saves 3-8 minutes in copying.

The Hunter is designed to be right on track — time after time — in copying fixed to removable media. Simply, the Hunter preserves the cartridge advantage by using a single fixed disk

MPETITION IN DUST.

servo surface to position on the cartridge disk. Seeks are faster and surer than the competition by a time factor of more than 13 to 1.

Our loader is really tops.

The Hunter cartridge receiver is as simple as can be.

Complex mechanisms with bearings, rods, plates and switches just aren't needed.

On the top-loading Hunter, gravity does the loading. And gravity behaves the same way time after time.

Score another point—a "scoreboard."

To avoid unnecessary service calls, the Hunter has a prominent front panel display that indicates operator or program errors plus malfunction information.

Made for fast "pit stop" service.

The Hunter utilizes self diagnostics and a modular component concept for fast, cost-effective servicing with a minimum of downtime.

For example, the power supply, power amplifier and transformer can be disassembled from the unit by removing only four screws. No de-soldering necessary.

Call now for your evaluation unit.

Full comparison details are available from your nearby Century Data sales office. Now is the time to pick your evaluation unit and compare us and them side by side.

Century Data Systems, 1270 N. Kraemer Blvd., Anaheim, CA 92806. Phone (714) 632-7111.

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CIRCLE 21 ON INQUIRY CARD

MARKSMAN REAC

20-microinch head flying height.

Low-flying Winchester technology isn't new, of course.

But the technology necessary to bring it to the micro/mini marketplace sure is.

Attaining and maintaining tolerances for accuracy like this while keeping the price down requires an all-out commitment of talent and resources.

The ultra-clean room facilities alone mind-boggle the uninitiated. Marksman units are assembled and sealed in a room so clean that excessive hand movement is prohibited because it creates five times the contamination of normal movement.

Century Data has made the commitment, solved the problems, kept a lid on the price, and is delivering Marksman products like never before.

If others are making you promises for the future, maybe you should take them with a grain of salt (roughly 600 times taller than our head flying height).

Daily production up, up and away.

If you think we're making a big production out of the Marksman, you're absolutely right.

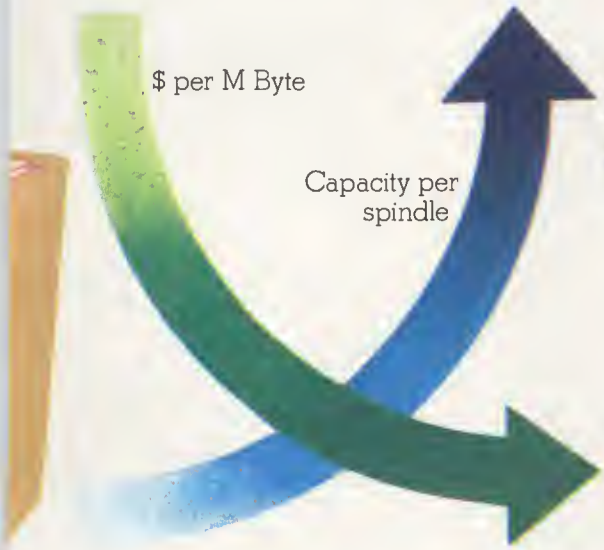
Marksman product is being delivered nearly as fast as orders are processed. Less than 30 days A.R.O. is commonplace.

When it comes to Winchester promises, Century Data delivers today.

HES NEW HEIGHTS.

Storage capacities going sky high, costs dropping to micro level.

The Marksman offers high-capacity storage at low prices. Its rock bottom cost-per-megabyte, along with access times only half those of conventional storage, make it an ideal alternative to floppies and other low-end memory products.



We're currently shipping both 10 MB and 20 MB versions, with a 40 MB model right on their heels and even more to come.

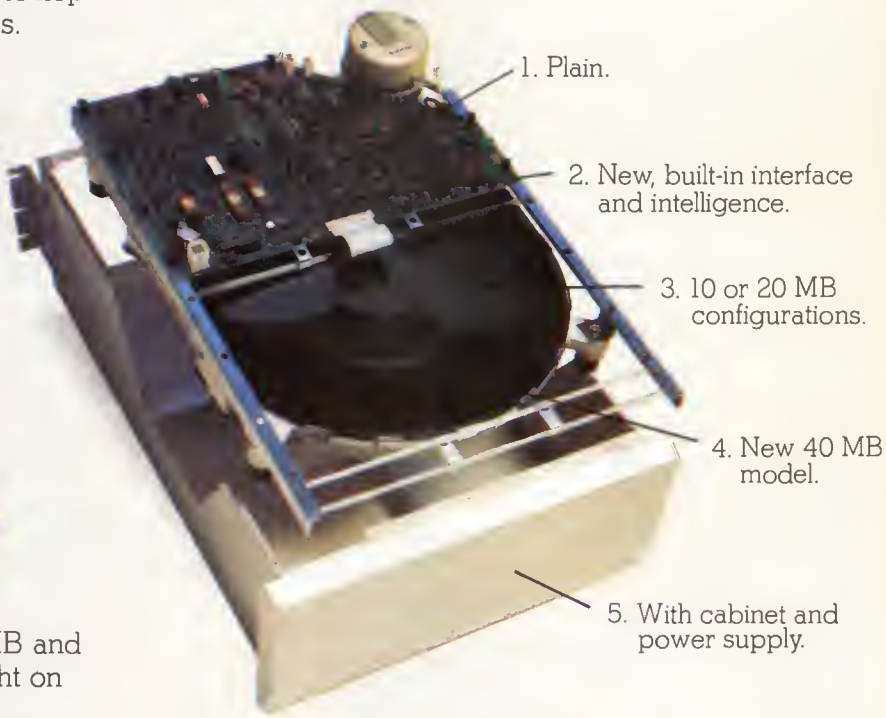
Pricing for the 40 MB Marksman is under $1800 in OEM quantities—actually less than projections on rumored smaller competitive units which will someday have only one-fourth the capacity.

High intelligence, room to grow.

To save you interfacing time and money, one Marksman model comes with a built-in microprocessor-based controller/formatter. It contains many of the interface and overhead functions normally relegated to the custom controller and CPU. That leaves you very little to do to put the whole system on-line.

It fills tall orders five ways.

You can order the Marksman plain or with everything on it.



See it tower over competition.

This Winchester is loaded. High reliability. Low price. Quick delivery. Wide variety of capacities and options.

Don't wait. Contact us today for all the facts. Century Data Systems, 1270 N. Kraemer Blvd., Anaheim, CA 92806. Phone (714) 632-7111.

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CIRCLE 149 ON INQUIRY CARD

add main memory, or add a fixed head disc.

The semiconductor disc is built using high speed, low power dynamic 16k RAMs, giving a storage capacity of from 12M to 72M bytes with maximum access time of 0.4 ms. Standard data transfer rate is 1.5M to 2.0M bytes/s depending on CPU channel characteristics and channel cable length. An optional 2-byte wide feature increases this rate to 3M to 4M bytes/s. Using controller options the system can be attached to as many as four channels to achieve transfer rate of up to 16M bytes/s.

An iSBC-86™ single-board computer in the system manages the IBM 370/303X channel protocol; it emulates the interface between 370/303X channel and 2835/2305 or 3830/3350 controllers/disc systems. The computer also transfers data to and from RAM storage and automatically formats the system to the required configuration at startup.

In addition the SBC-86 performs continuous preventative maintenance on the system. Cycling through the unit, it reads, corrects if necessary, and rewrites data. When a correctable error is found, the computer corrects it and records the board location in its own memory for future reference. Whenever it finds a predetermined number of errors in a given area, it automatically transfers the contents of that area to spare storage within the unit. Subsequent addressing is redirected to the spare area and an external indication is given of the failure so that the board or chip may be replaced during regular maintenance.

Double-bit error correction logic in the system provides a level of data security normally found only in military equipment. As a further check on data integrity, a 48-bit CRC code is appended to each data record.

Another function of the integral computer is to format storage to conform to either 2305 or 3350 track specifications and create label and volume table of contents (VTOC). If a paging data set resides on the 3805, the computer allocates and formats the paging file to conform to the host operating system requirements, and enters the data set name into the VTOC. This automatic storage formatting facilitates interfacing and decreases the time required for initialization.

If the system is emulating a 3350, the microcomputer calculates the difference between storage available and capacity of a 3350, then enters a dummy file into the VTOC to account for missing space.

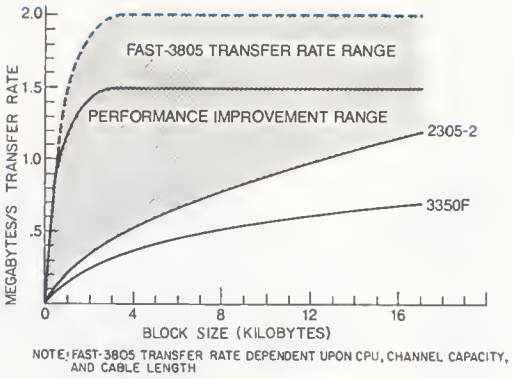
Standard system contains one controller; three others can be added. The 2305 extended storage feature allows the logical equivalent of more than two 2305s (22.4M bytes) to be attached to a single controller. Although the optional extended channel cable length allows the system to be placed 200 ft (60 m) from the channel, some degradation will occur.

A 2-channel switch allows any controller in the system to be shared between two channels, and allows a single system to be accessed by up to eight channels. A 2-byte wide feature lets two bytes be transferred in the same time as one on the standard controller, doubling the transfer rate to 3M to 4M bytes/s.

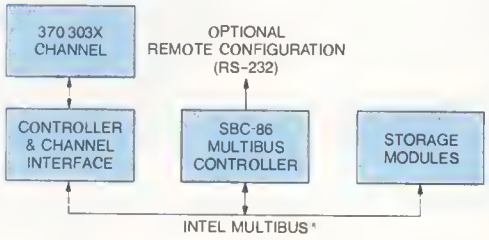
The standard unit is 72 x 60 x 30″ deep (183 x 152 x 76 cm) and is cooled by a fan circulating 1800 ft³ (51 m³)/min. Basic storage modules (up to eight) each contain one buffer card, backplane, and storage cards having 9M bytes/module. Two motor generator sets provide power to eliminate loss of data in case of momentary power fluctuations. A battery option protects data for up to 12 min in case of complete external power failure.

A typical configuration consisting of one controller and 12M-bytes storage sells for $130,500. A system with 2-byte wide feature, two channel switches, and 48M-byte capacity has a price of $507,920. These prices are 80% and 69%, respectively, of those for similar capacity IBM configurations.

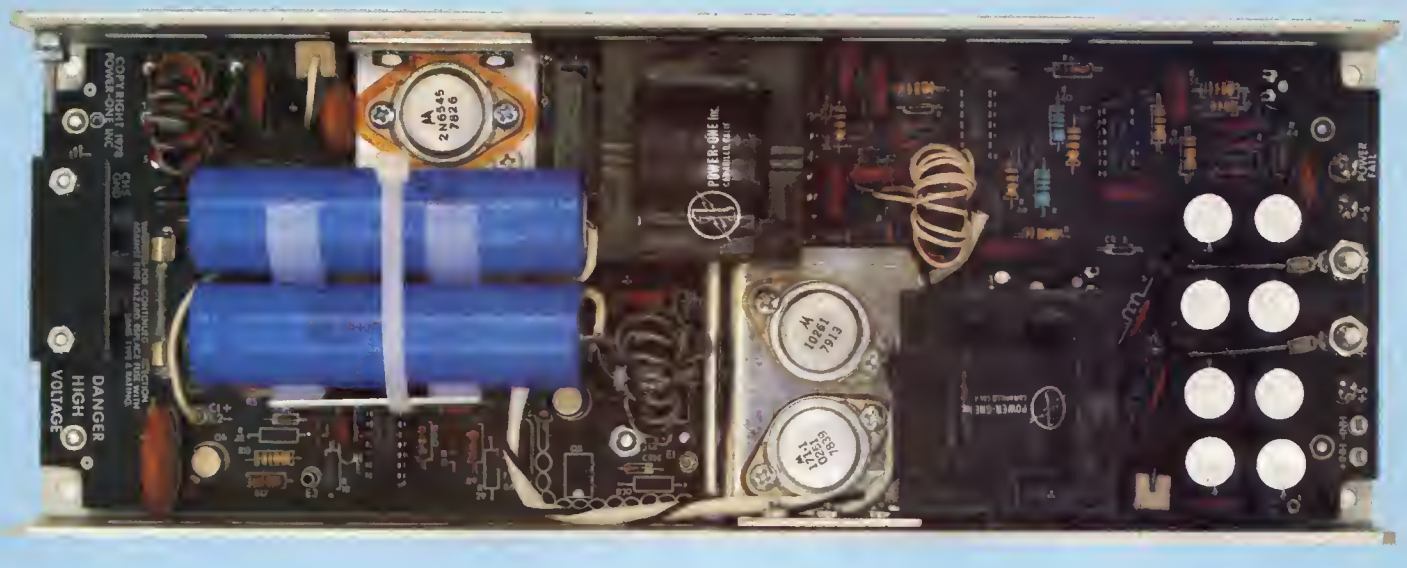
Circle 178 on Inquiry Card



Using 1.2M-byte/s transfer rate, 4k block size, and single-byte wide transfer, Intel's FAST-3805 semiconductor disc is 3.5 times faster than IBM's 3350F disc system and twice as fast as 2305-2. Steep climb in 3805 curve is due to unit's 0.4-ms access time



FAST-3805 semiconductor disc holds up to 72M bytes and two controllers. Internally system is organized around SBC-86 computer and Multibus. Optional RS-232 port allows attachment of remote configuration console



IT TOOK POWER-ONE TO DO IT...

a switching power supply as dependable as a linear.

When Power-One decided to build a switching power supply, we issued one simple mandate: it must be as dependable as our linears. Well, we did it. A direct drive 5-volt 40-amp switching power supply that's smaller, lighter, simpler, more reliable and less expensive than the rest.

Direct Drive Switching

By using a self-driven switching stage, we've done away with the starting bias, drive and the current sensing transformers. A big reduction in weight plus lower cost, more precise drive control and fewer input to output noise paths. To assure maximum protection against AC line transients and fluctuations, a unique "volt-second" regulation circuit is employed.

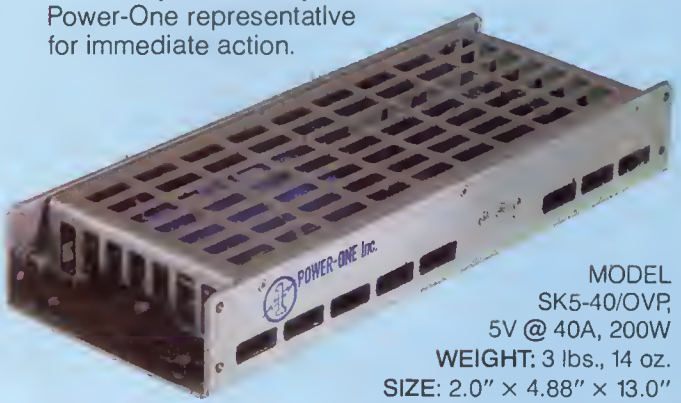
Safeguard Design

We've built in a number of safeguards. Like our digital feedback system which yields exceptional loop stability while maintaining positive control of critical switching parameters. And a unique anti-saturation circuit to protect the power transistors from the dire effects of transformer saturation. Plus, by putting inputs at one end of the supply and outputs at the other, we've eliminated inter-circuit cross talk. And speaking of inputs, our dual range design permits either 115 or 230 VAC operation without changing jumpers.

The Bottom Line

Switching frequency: 28KHz — stable as a rock. Size: a mere 4.88 × 13 × 2 inches — more watts to the inch and more power for the buck. The price: $250 for single units.

Send for complete details. Or better yet, contact your local Power-One representative for immediate action.



MODEL
SK5-40/OVP,
5V @ 40A, 200W
WEIGHT: 3 lbs., 14 oz.
SIZE: 2.0" × 4.88" × 13.0"
PRICE: $250 Single Quantity

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CIRCLE 22 ON INQUIRY CARD

The SA800 and the SA850.
Whether you use our SA800/801, the world's most demanded floppy disk drive, or our SA850/851—the world's first IBM-compatible, double-sided, double density disk drive—you're sure to get ahead. Why? Because only Shugart controls the head technology that gives you the best ceramic read/write heads on the market. And our OEM's know that they are buying the latest technology, because Shugart is the only independent company in the business which controls its own head R&D and manufacturing. That's why we're the only company in the business to have delivered over half a million of these heads.

Two great ahead with

Why the SA800/801 is the industry standard. It's no secret that the SA800/801 floppy drive has become the industry standard. Its performance results directly from our proprietary head technology. When you talk about a media life of over 3.5 million passes and a head life that exceeds 15,000 hours, you're talking about standard-setting performance. Add to that a choice of 400 kbytes or 800 kbytes (unformatted) and single or double density capability on the same drive for the same price. And then settle the matter with system performance like soft read error rates of $1/10^9$, hard read errors of $1/10^{12}$, and seek errors of $1/10^6$.

The SA850/851. First and first with Fasflex™
Which means the SA850/851 double-sided floppy is the first independently manufactured drive to double data storage capacity. And it's the first to cut access time to 3 milliseconds with the Fasflex™ actuator. And the SA850 offers maximum media flexibility, too. Storage? A double-sided, double density SA850 gives you up to 1600 kbytes (unformatted). It can utilize FM, MFM, or M²FM encoding. Access time? Shugart's proprietary Fasflex metal band actuator gives you a 3ms track to track access time with an average seek time, including settling, of 91ms. Yet Fasflex requires only half the power of lead screw actuators. Media flexibility? Whether you use conveniently obtainable Shugart media, or other brands, the SA850 drive family reads and writes data on single and double density media, and on single and double-sided media.

ways to get Shugart.

Two out of three OEM's specify Shugart. During 1979, more than a quarter million Shugart floppy disk drives will be installed throughout the world. No other manufacturer comes close to that magnitude of delivery. The reason? OEM's rely on our total commitment to R&D. That commitment means we deliver state-of-the-art, low cost, rotating memory products that have a track record for quickly becoming industry standards. Our success comes from our grasp of where performance in low cost, rotating memory originates: the head technology. That's our strength; it's why we're called The Headstrong Company. Shugart Associates Headquarters: 435 Oakmead Parkway, Sunnyvale, California 94086 (408) 733-0100; West Coast Sales/Service: (408) 737-9241; Midwest Sales/Service: (612) 574-9750; East Coast Sales/Service: (617) 893-0560; Europe Sales/Service: Paris (1) 686-00-85; Munich (089) 176006; Shugart products are also available off the shelf from local Hamilton Avnet outlets.

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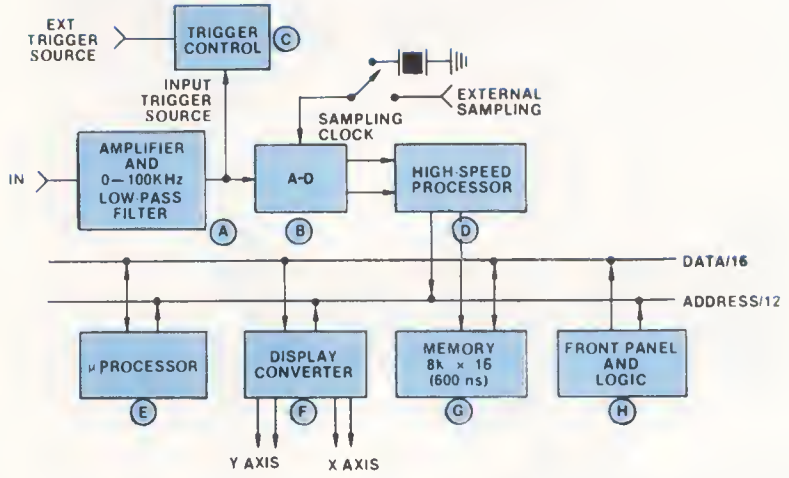
CIRCLE 23 ON INQUIRY CARD

Plug-In Spectrum Analyzer Combines Simplicity With FFT Performance



Key hardware elements in Rockland System's 7530A spectrum analyzer are (A) low noise, high sensitivity amplifier and 120-dB/octave low pass filter; (B) 12-bit linear A-D converter; (C) trigger control; (D) CPU that first bandpass filters input signal and then performs FFT spectrum analysis on it; (E) CPU that interprets front panel controls; (F) display converter; and (G) 8k x 16-bit memory formed from 16k-bit chips

A general purpose spectrum analyzer, the 7530A provides quantitative analytical capability of FFT based spectrum instrumentation in a compact plug-in module. In designing the unit, Rockland Systems Corp, Rockleigh Industrial Pk, Rockleigh, NJ 07647, reshaped most major elements of a classical analyzer. Configured as a plug-in module for Tektronix® series 7000 oscilloscope mainframes, the analyzer combines the simplicity of a swept tuned analyzer with the high performance of an FFT based design, including 1-Hz resolution at 100 kHz, and 90-dB dynamic range at rated accuracy with a -160 dB/$\sqrt{\text{Hz}}$ noise floor.

Among the developments incorporated into the design are an "extra dimension" in display resolution: the entire 0- to 100-kHz spectrum is always displayed as a background on the scope screen, at low intensity; a manually selected, intensified segment shows the part selected for detailed study. This segment is displayed as an expanded, full-screen-width presentation, at full intensity, in the foreground. Directly calibrated measurements are provided of every point (amplitude and frequency) on every spectrum displayed, in volts, power density, dBV, and dBR (relative to selected reference). The architecture incorporates a second separate computer (not the one used for high speed signal processing to achieve the Fourier transformation) to monitor control settings, manage display, and interpret what has been set up. Algorithms, which sharply reduce hardware costs, provide fast settling smoothing performance, and permit the operator-to-processor interface to be computer automated. In essence, the unit is a special purpose digital computer with analog

FINALLY. A FIBER OPTIC LINK YOU CAN TAKE SERIOUSLY.

Introducing the first data link that features low cost, versatility, and high performance.

$49.95 per module and Sweet Spot™ LED

Our unique Sweet Spot design lets you couple to a variety of cables including Siecor, Galite and Dupont plastic or glass.

SPX4140—TRANSMITTER

SPX4141—RECEIVER

2 kilometers transmission at 10 Mb/s(min) with 10^{-8} BER

LED performance this powerful opens the door to unlimited application ideas. And since the modules are a compact .5''x.5''x 1.3'', they're easy to design into existing systems.

Full microcomputer compatibility

True TTL compatibility, 0° to 70°C operation, and a 5 volt unregulated power requirement are important features. But state-of-the-art IC design also provides single line, self clocking, optical data transmission at maximum rated performance.

The Missing Link

Now you can evaluate all the features of our modules through our special fiber optic kit, The Missing Link. It contains modules, connectors, terminated cable and instructions. All for $495.

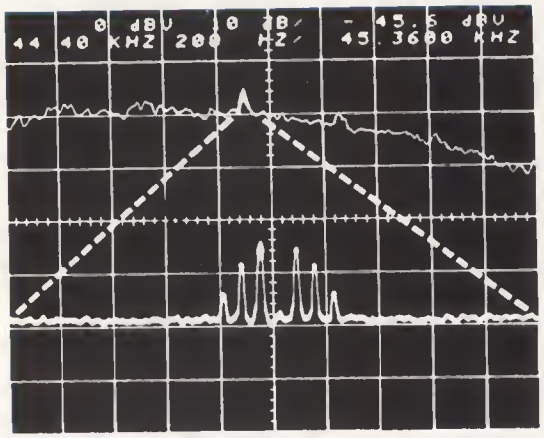
Or, if you have bigger plans, you can order modules in 1000 lot quantities for $49.95 each.

From Spectronics, the fiber optics leader

If that sounds impressive, it should. Because Spectronics is the only company advanced enough to take this technology to the production stage.

Ask your Spectronics distributor for The Missing Link, or contact Spectronics for information at 830 East Arapaho Road, Richardson, Texas 75081; Telephone (214) 234-4271.

Spectronics
A division of Honeywell



Display generated by 7530A presents at all times entire spectrum, analysis window width and starting frequency, window only zoomed to full width, and all parameters of every element in either spectrum in direct reading calibrated alphanumeric readouts

interfaces for signal acquisition and oscilloscope display control.

Using a high speed spectrum processing computer over the frequency range from dc to 100 kHz, the components of the Fourier spectrum are quantitatively measured, computed as a true power spectrum, and displayed at deliberately reduced intensity. The "analysis window" selected for detailed examination is recomputed, and presented at full intensity. Both spectra have 200-line resolution.

A manually positioned cursor and associated controls provide accurate readout of amplitude and frequency for any selected point on either the foreground or background display. Absolute (dBV, dBm), relative (dBR), or spectral density (RMS/$\sqrt{Hz}$) readings are selectable, and are displayed at the top of the CRT presentation as alphanumeric readouts. Also displayed are the frequency of the cursor in Hertz, relative time of cursor in seconds, vertical and horizontal axis calibration, and start frequency of the display window.

Frequency accuracy of the unit is ±0.001%; sensitivity accuracy is 10 dB/step ±0.2 dB, 0.32 Vrms to 10 Vrms full scale calibrated, to 32-Vrms full scale uncalibrated. The linear dynamic range is ±0.1 dB or ±0.001% (whichever is greater) down to 70 dB below full scale (to 90 dB below full scale under certain conditions). Spurious signals are more than 70 dB below full scale: harmonics are down 75 dB, typical; intermodulation products are 80 dB below full scale.

Circle 179 on Inquiry Card

Microprocessor Based Units Expand Commercial Computer System Family

An integrated multiterminal business system, the CS/30 uses an interactive version of the COBOL programming language. Capable of maintaining more than 20M bytes of information, two models of the microprocessor based systems are designed to minimize the costs of system acquisition and applications software development. Data General Corp, Rt 9, Westboro, MA 01581 has aimed the machines at small companies of up to 50 employees or for use as part of a distributed processing network within large firms.

CS/30 Mod C1 has a microprocessor with 64k bytes of MOS main memory, one 10M-byte cartridge disc, Dasher CRT console and interface, and choice of printers ranging from 60 char/s to 300 lines/min. Mod C3 will support an additional 32k bytes of main memory. This offers a total memory capacity of 96k bytes and allows the unit to support up to three active CRT terminals. Options for both systems include a second 10M-byte cartridge disc drive, 315k-byte diskette drive, and IBM 2780/3780 compatible synchronous communications capability.

System compatibility extends through the entire CS family and includes the ICOS operating system, Interactive COBOL language, and communications capabilities as well as all program levels and sequential, relative, and indexed sequential access method file levels. The ICOS operating system has been enhanced to facilitate program development.

Enhanced editing capability for the Interactive COBOL editor have been added as well as a COMPUTE verb that allows multiple arithmetic and exponential functions to be expressed in a single statement, and an enhanced interactive screen formatter that automatically generates necessary program code. An added inquire utility allows users to browse through ISAM files to add, delete, or update data. A collapse utility allows index levels to be condensed for more efficient retrieval.

A basic configuration Mod C1 that includes 64k-byte memory, CRT console and interface, 10M-byte cartridge subsystem, and 60-char/s RO printer sells for $21,090. A midrange C3 with 80k-bytes memory, console/interface, CRT, 10M-byte disc, and 180-char/s LP2 printer has a price tag of $25,930.

Circle 180 on Inquiry Card

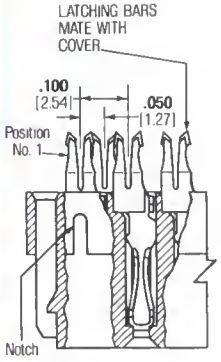
Realtime, Interactive Digital Image Processor Operates Standalone

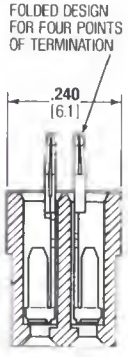
The Vision One/20 digital image processor combines up to 134M bits of image refresh data base memory, firmware resident operating system, and integral microprocessor controller to provide photographic quality images on a high resolution raster monitor. Operating on a realtime interactive standalone basis, the system from Comtal Corp, PO Box 5087, Pasadena, CA 91107 processes images stored in analog form on film or in digital form from sensors and scanners.

Up to 134M bits of random access image refresh memory offers capability to support up to 64 images of 512 x 512 picture elements (pixels), upgrading the display to 1024 x 1024 pixels redefines the number of

"Look, I've got two challenges for my ribbon cable interconnects— to reduce manufacturing rejection rates and prevent contact damage during testing. Got any solutions?"

AMP Latch.





Some facts worth knowing about AMP Latch Connectors

Function: Simultaneous mass termination of all conductors without cable stripping.
Wire types: Small gauge solid or stranded discrete wires as well as flat ribbon, woven ribbon and other types flat cable with round conductors on .050" centers.
No. of positions: 10 to 60.
Connector types: Wide variety of cable-to-cable, card edge, DIP and receptacle connectors available.
Mates with: Full range of AMPMODU headers and pcb posts.

Electrical Current Rating:
1 Ampere (Continuous).
Operating Temperature Range:
−55°C to +105°C.
Dielectric Withstanding Voltage:
500 Volts, RMS.
Tooling available: Pneumatic and Manual Bench Mounted Models and a Hand Tool, each with interchangeable die sets.
Who to contact: Call AMP Latch Information Desk at (717) 564-0100. Ext. 8400. Or write AMP Incorporated, Harrisburg, PA 17105.
Product Information: Check Reader Service Number 99.

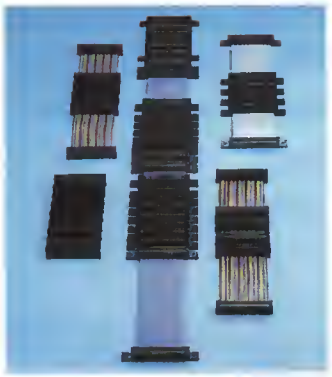
As fast as you can say "downtime" your production, test or repair people can activate an AMP Latch Easy Release Header with one hand. Just squeeze and the cable half is disengaged. No wrenching on the cable. No wiggling. And no damaged contacts. An important matter when

We sure do.

neither your production costs nor your on-board costs can take a back seat to one another. And one of many reasons why AMP Latch has drawn the attention of designers in the data processing, instrument and communications industries.
Yet AMP Latch offers a unique feature that extends far beyond what other ribbon cable connectors can offer. It offers precision registration built into the tooling which minimizes rejection rates.
Unquestioned reliability. That's what AMP Latch is about, too. You get a four-point electrical contact and mechanical grip for each conductor.
Built-in inspection ports make test simpler than ever.
The fact is, nobody today has a wider range of easy-to-apply no-strip, no-solder, round conductor flat cable connectors than AMP.
For more details, see the opposite page and the page overleaf.

AMP has a better way.

And cost effective tooling.



With AMP Latch Tooling the terminations are made quickly, easily and simultaneously. No need for pre-stripping the insulation. One tool will terminate virtually all popular round conductor flexible cable, including those with flat side down or ribbed side down.

Two basic bench-mounted AMP Latch tools include: a heavy-duty pneumatically powered unit and a manually operated unit. Both are reliable. Both are easy to load. And precision cable registration is built in. Alignment is automatic and positive. Six different precision die sets are available for terminating receptacle, plug, card edge, paddle board and pin connectors as well as discrete wire.

Also available is equipment for daisy chain terminations, and a hand tool with interchangeable dies.

For the complete story on AMP Latch Connectors, AMP Latch Tooling, and the AMP Technical Support that goes with them, call AMP Latch Information Desk at (717) 564-0100. Ext. 8400. Or write AMP Incorporated, Harrisburg, PA 17105.

AMP

images stored to 16. The images are 8 bits deep for black and white and 24 bits deep for color (8 bits each for red, blue, and green). High speed RAMs and memory architecture allow the user to overview images as large as 4096 x 4096 x 8 bits deep.

This refresh memory stores images in digital data form—one byte for each pixel in black and white and three for each color pixel. There are 256 shades of gray and 16 million possible colors for every pixel. With a cycle time of 800 ns, the refresh memory runs at 10M pixels/s in a 512 x 512 pixel system. Multiplexed, it runs at 40M pixels/s.

An LSI-11 microcomputer manages memory, handling the switching and control of high resolution graphic arts images. It also controls processing and display functions, providing various measurements within an image for specific analysis needs. Since the computer is an integral part of the system, instructions access the memory directly and are executed instantly, eliminating the time consuming instruction I/O encountered in systems where the computer is separate from the display.

Memory management facilitates the handling of high resolution color graphic art imagery, multiple station monochrome reconnaissance imagery, and multilevel raster color graphics. It also lets the service engineer remove boards for repair or add blocks of memory; the system automatically senses which boards are connected online and dynamically allocates them for most effective use.

Pipeline processing logic (one set for each of up to four user stations) recomputes all picture elements in the monochrome or true-color viewing window in 0.033 s, and permits partitioned or shared use of the dual-ported RAM. Typical pipeline processing functions include changing brightness, sharpening an image, arithmetic operations, color encoding, roam, and zoom. Internal processing speeds allow over 70M operations/s for realtime convolution and zooming. Freeze frame feedback allows user programmed iterations for more powerful spatial filtering as well as larger zooming. Dual porting of the memory allows image loading and display on a non-interfering basis.

Resident in the LSI-11, the operating system includes 100 high level graphics and image manipulation commands in firmware. The commands manipulate the image frames; no host software is needed. Instruction programming, linking (macroinstruction sequences), and execution in software are all implemented via initial letters on the keyboard.

Presentation commands allow the system to combine images for display and add graphics for labeling, outlining, and overlay; utility commands allow keyboard programming, linking, and chaining of instructions for macroinstructions and execution; and I/O commands permit image transfer to and from the system via interface options.

Memory management commands permit users to define their image size and depth (ie, monochrome or color), scratch images, and memory allocation. Pipeline processor commands permit brightness corrections, analytical function loading, pseudo-color control, and dynamic brightness correction adjustment, as well as roaming, zooming, image arithmetic combination, and convolution implementation.

Circle 181 on Inquiry Card

Minicomputer and Cache Add Performance to Distributed Systems

Compatible extensions to the existing DS990 family of distributed computing systems, models 20 and 30 provide fast throughput and access to large data bases. The 990/12 minicomputer, on which these systems are based, offers three times the speed of the /10. The application of advanced technology and the cache memory system are cited by Texas Instruments Inc, Digital Systems Div, PO Box 1444, Houston, TX 77001 as factors contributing to this increase.

Basis of the systems, the 990/12 minicomputer incorporates 16-bit words, memory to memory architecture, 16 workspace registers, mapping to 2M-bytes of memory, 72 basic instructions, word and byte operations, 16 interrupt levels, error correcting memory, and high speed TILINE multiuser bus. Performance improvements are achieved by the use of overlapped operations, faster LSI devices, CPU workspace cache, TILINE cache option on memory, and improved memory cycle. Other features include 71 additional instructions, an error trace memory, and extended memory protection.

The cache controller utilizes 2k bytes of 350-ns memory. Whenever the processor executes code out of cache instead of main memory, the cycle time of the processor approaches 380 ns. Main memory cycle times are 740 ns.

Both models share software compatibility as well as peripherals with DS990 models 4, 6, and 8. All use the DX10 operating system, and high level languages include BASIC, COBOL, FORTRAN, Pascal, RPG II, TIFORM CRT management, and database management system.

In a minimum configuration, the model 20 includes 256k bytes of error correcting memory with a 2k-byte cache controller, two model 911 video display terminals, 50M-byte DS50 disc, and choice of magnetic tape or second disc. The 990/12 CPU is packaged in a 17-slot enclosure with a 70" (178-cm) rack cabinet. This system expands to include 20 terminals and 4 disc drives.

Using the 990/12 processor, 17-slot enclosure, and 70" (178-cm) rack cabinet, the model 30 contains 256k-bytes of error correcting memory with 2k-byte cache controller, two 911 video display terminals, 200M-byte DS200 disc, and choice of magnetic tape or additional disc. This system expands to include 20 terminals and up to 4 discs.

Prices are quoted as $19,598 for a 990/12 computer with 256k bytes of memory without cache and $22,948 with cache, in quantities of 25. A minimum configuration DS990 model 20 with magnetic tape backup sells for $64,500; and a minimum model 30 for $77,400. Deliveries are scheduled for fourth quarter this year.

Circle 182 on Inquiry Card

Portable Oscilloscope Upgrades Measurement And Display Capabilities

Performance and features of the 465B 100-MHz portable oscilloscope meet the measurement and display capabilities required by high performance digital circuitry. While maintaining the price and features of the 465, Tektronix, Inc, PO Box 500, Beaverton, OR 97077 has added flexible vertical control modes, simultaneous trigger view with zero delay, and 2-ns maximum magnified sweep speed.

In addition to the 100-MHz at 5-mV/div, dual trace, delayed sweep, and 8 x 10-cm CRT of the 465, the 465B has "push-push" vertical mode selection buttons that allow the operator to choose channel 1 and/or channel 2, differential, and a trigger view in any combination. The ability to look at both channels, their sum, and the external trigger simultaneously provides a complete picture of the measurement.

Electronic switching between intensified and delayed sweep adds convenience. In alternate mode the operator can look at both A sweep and B sweep simultaneously with no need to switch back and forth between modes or reposition a mixed sweep display. For greater ease in examining fast risetime waveforms, a 2-ns/div maximum sweep speed is standard. This increase permits examination of fast risetime signals like critical clock edges. The use of low noise IC technology devices in the unit provides a sharper trace, and LED panel indicators improve reliability and eliminate operator errors.

Circle 183 on Inquiry Card

Information Processing System Uses Hardware and Software Tailored for Job

Three progressive building block approaches to word processing, data entry, and specialized application systems are offered by the System 84 Information Processor. Introduced by 3M Co's Business Communication Products Dept, PO Box 33600, St Paul, MN 55133, software packages offer varying levels of sophistication and a custom language for hardware specifically configured to the task.

Hardware configurations and options for the display based System 84 processor include up to four disc drives, 660-word/min printer, view mode video screen, and OCR, magnetic card, magnetic tape, and communications. A sheet feed option feeds up to 180 sheets of paper to the printer automatically, eliminating tedious paper insertion operations and allowing unattended printing.

Filling word processing needs, Level 1 software encompasses basic entry level text editing functions and offers draft, revise, playback, print/while, search and replace, and headings and footings. Level 2 takes care of list management and letter writing applications providing capability for form letters, document assembly, envelope typing, name and address list sort, and parallel print/extract. For publications work, Level 3 adds math text, proportional spacing, and multicolumn features to those of Levels 1 and 2.

For use in data entry applications, the CL_6 language encompasses six major functions to allow programming flexibility. Written in CL_6 for use in consumer affairs/response departments, the Consumer Communications System provides personalized communications as well as management reports categorizing and classifying incoming correspondence. Reports can include correspondence summary report, complaint report, and financial summary report.

Circle 184 on Inquiry Card

"Choosing Intel gave us a twelve month jump on the competition."

Dr. Wang: "We were first with a unique, new approach to word processing—using microcomputers to implement distributed intelligence in multiple station systems. That approach has enabled us to increase our market share 50% a year in a market that's growing 40% a year. This year our word processing sales will pass $100 million. In 1974 they were just $9 million.

"We decided on Intel's 8080 microprocessor for our distributed logic system. Only Intel offered PL/M, the microcomputer programming language we needed to get our software written quickly. So quickly that we introduced our system a year ahead of any competition. And Intel's tools for programming have continued to help us offer our customers the high quality software they expect from Wang."

Intel's extensive microcomputer design tools have helped hundreds of companies just like Wang Labs capture the marketing advantage with Intel microcomputers and semiconductor memory.

Our Intellec® Microcomputer Development System makes it possible and profitable for companies like yours to take full advantage of the promise and potential of the microcomputer. For example, the world's most advanced microcomputer, our new 16-bit 8086, is the first and only 16-bit microcomputer supported by a high-level programming language—PL/M, part of the total 8086 software development package available for the Intellec system.

To begin writing your own success story, contact Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051 408/987-8080.

Intel's Intellec® Development System

intel® delivers.

Introducing the Sperry
Designed exclusively for three

The Sperry Univac V77-800 Miniframe is the newest and most powerful mini we've ever built—a high performance, multi-use, general-purpose minicomputer system designed for both commercial and scientific data processing. It has a memory range from 128K bytes to 2 megabytes (with error correcting memory) and a 150 nanosecond CPU with integrated cache of 1024 bytes. Plus 12K bytes of user programmable writable control store.

There's an optional new high speed 64-bit floating point processor that works in conjunction with a new globally optimized ANS '77 FORTRAN.

No wonder our three most important customers think so highly of it.

OUR OEM CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

The Miniframe is customer microprogrammable. So an OEM can implement his own firmware packages. And with the many software packages we offer, the OEM can add all the bells and whistles he wants.

The Miniframe comes with our largest instruction set ever. So OEM's with their own software have much more flexibility in design.

The Miniframe speaks PASCAL, the powerful new language for scientific, commercial, and system programming that most competitive systems still can't speak. And of course, it also speaks COBOL, FORTRAN and RPGII.

More good news is that the Miniframe is compatible with the rest of the V77 product line.

OUR SYSTEM HOUSE CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

Naturally, system houses want all the features OEM's do. And more.

So we gave them more.

More operating systems, for example. Choose from VORTEX or our new SUMMIT—an interactive, multi-terminal system with transaction processing and data base management. It gives you easy editing, screen formatting, and documentation aids. Plus speedy, comprehensive program development.

System houses also think PASCAL is important. Because it's more efficient, easier to maintain, expand, and modify.

The Miniframe brings systems builders a new query language called QL-77. It features inquire and report facilities. And interfaces

Univac V77-800 Miniframe. of our very best customers.

directly to TOTAL*, the data base management system. So preprocessing and intermediate handling are a thing of the past. Finally, TOTAL also gives you complete data base access and file access security.

OUR END USER CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

Take all the features we designed in for OEM's and system houses and say ditto for the end user.

But we didn't stop there. We also pressed a few special hot buttons just for end users.

Consider QL-77, for example. End users will love our new query language because it reduces the amount of application programming. By storing query language procedures right in the data base file. Where they can be easily and quickly recalled and executed at any time.

Once again, SUMMIT, our new operating system, helps the end user handle transaction processing. Without any additional, expensive software. It's also the right answer for a multi-tasking, "fully-implemented" distributed processing system.

Finally, the Miniframe supports DCA and conventional protocols. So you can talk to both SPERRY UNIVAC and IBM hosts.

YOU'LL KNOW WE DESIGNED THE MINIFRAME JUST FOR YOU.

No matter what your application, no matter what your need, the Miniframe may just be the answer.

For more information, write to us at Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, Irvine, California 92713. Or call (714) 833-2400, ext. 536.

In Europe, write Headquarters, Mini-Computer Operations, London NW10 8LS, England.

In Canada, write Headquarters, Mini-Computer Operations, 55 City Centre Drive, Mississauga, Ontario, L5B 1M4.

We're Sperry Univac.

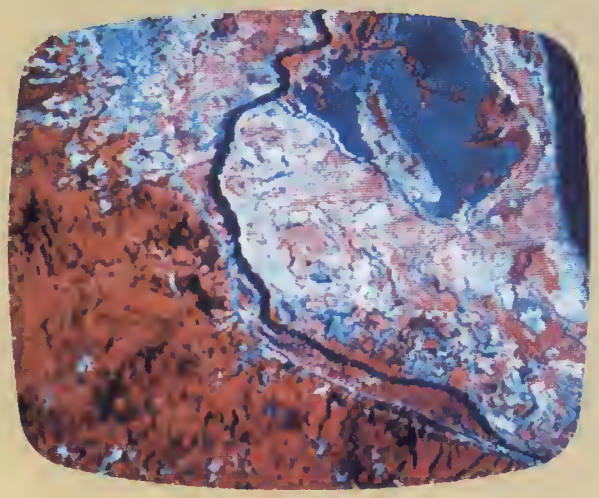
And our new Miniframe is going to solve some very big problems.

SPERRY UNIVAC

SPERRY UNIVAC IS A DIVISION OF SPERRY RAND CORPORATION

*TOTAL is a registered trademark of Cincom, Inc.

Image processing. Your way.



Now, with the Grinnell GMR-270 Image Processing System, you can have pipeline image processing tailored to fit your application.

The GMR-270 combines the best features of our proven GMR-27 line of high speed graphic display systems with a special package of sophisticated image processing features. The result is a modular image processing system that can be furnished with any or all of the following:

- Convolution
- Image multiplication and ratioing
- Image arithmetic operations
- Zoom and pan
- Up to four 8-bit image memories
- Function memories
- Pseudo-color tables
- Video digitizers with frame averaging
- Split screen and image toggling
- Full graphics and alphanumerics
- Up to four overlay memory planes
- Independent cursors
- Trackballs and joysticks
- External synchronization
- Plug compatible interfaces for most minicomputers

In addition, the GMR-270 has a display resolution of 512 x 512 pixels and a video format that is RS-170 compatible. It is housed in a rack-mountable chassis and drives standard TV monitors.

Besides the GMR-270, Grinnell manufactures two complete lines of graphic television display systems: the GMR-27 Series and the GMR-37 Series. GMR-27 units are high speed, graphic and image display systems; GMR-37 units are low cost graphic display systems. Both are available with display resolutions from 256 x 256 to 1024 x 1024.

So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a system that can do it. For detailed specifications and/or a quotation, call or write today.

GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920

CIRCLE 29 ON INQUIRY CARD

Keyboard Terminal Module Implements Digital Logic On Single PC Board

With a full ASCII keyboard and all the logic circuitry for a full keyboard terminal on a single PC board, KTM-2 Tubeless Terminals also provide a display interface that offers composite video for user supplied monitor or standard TV equipped with rf modulator. Developed by Synertek Systems Corp, 150 S Wolfe Rd, Sunnyvale, CA 94086, the units incorporate 8 MOS LSI chips, including two dedicated microprocessors, and use 20 TTL devices.

Use of standard LSI devices results in a cost-effective design with flexibility for accommodating custom applications, and provides more features at low cost than the use of CRT controller chip. The two 6500 series microprocessors offer the flexibility to implement user defined character set and field size, control character protocol, screen organization, and keyboard layout.

The ASCII board provides facilities for 24 x 40-char screen size, full upper and lower case alphanumerics with descenders, control and special characters, and 128 graphics characters. Display features include reverse video, scrolling, cursor blanking, and full cursor control.

Two full duplex serial communication ports transmit at selectable rates from 110 to 9600 baud. The main port is used primarily with a computer for information transfer, the auxiliary port with a printer for hard copy.

The terminals are available as the KTM-2 without case and 5-V power supply, or as the KTM-2/80, an 80-column version. Prices are $349 and $424, respectively.

Circle 185 on Inquiry Card

Key to Disc System Offers Increased Storage and Communications

An enhanced version of the computer assisted data entry (CADE) shared processor key to disc system, the 1900/10 offers larger main memory, increased disc storage capacity, larger CRT display, station printers, and communication in IBM 3270 interactive protocol. By implementing these features, Sperry Univac, PO Box 500, Blue Bell, PA 19424 has enabled the systems to work in a 3270 network and to access the data bases in IBM host processors.

Main memory in the unit expands from 128k to 512k bytes in 128k-byte increments. Disc capacity increases to 200M bytes in two phases. The first provides an increase to 70.4M bytes and the second phase raises capacity to 200M bytes.

Larger screen capacity for the CRT allows 2000 characters to be displayed on 80-character lines. Record lengths up to 999 characters can be handled by the system. This increase in screen capacity avoids the need to reformat information received when interfacing with an IBM 3270 environment.

Capability of operating under the IBM 3270 interactive protocol environment allows the system to operate in the same network with 3270 terminals without major changes to the host processor. Other system features include COBOL subset and data capture checkbox formatting, which make the system programmable by persons unfamiliar with data processing. The database management system supports high speed keying and emulates the benefits of online data entry.

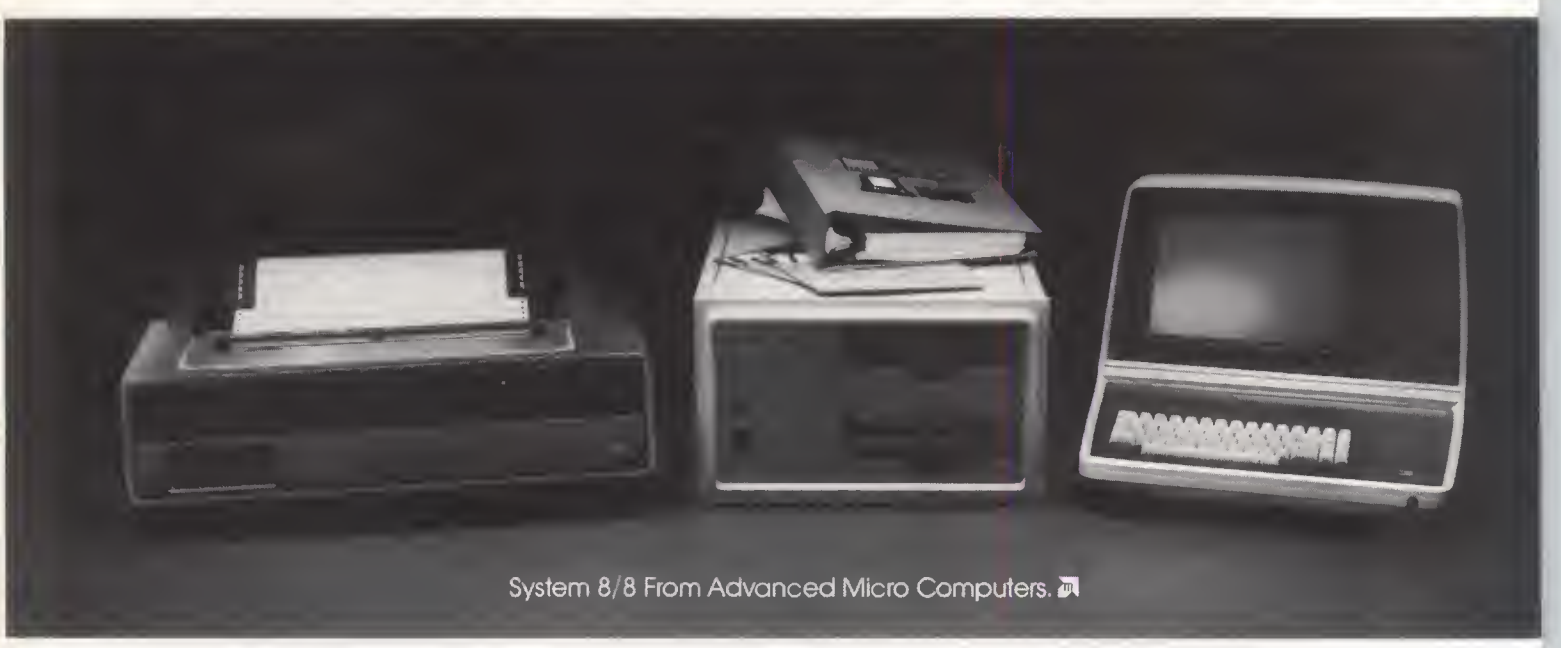
Circle 186 on Inquiry Card

You've compared the AmZ8000 with the 8086. Now you know what we know. The AmZ8000 is the best 16-bit CPU.

But if you're still a little worried about support, don't be.

Advanced Micro Devices Announces System 8/8.

System 8/8 was designed especially to support the AmZ8000 in both hardware



Advanced Micro Computers is a subsidiary of Advanced Micro Devices.

"OK, the AmZ8000 is better. But what about support?"

and software development. But thanks to its multiple-master bus structure, System 8/8 also supports the 8080, 8085 and Z80. It's the only upgradeable, expandable development system you can buy.

The basic machine comes with 32K bytes of RAM, two floppy disk drives, an RS232 serial port, six 8-bit parallel ports and an Am9080A main CPU.

And along with all that powerful hardware, you get an equally powerful set of software.

There's an AmZ8000 translator and macroassembler, a terrific text editor, 8080 macroassemblers, a linking loader and a dynamite debugger. Plus a very sophisticated disk operating system that provides rapid access to programs through a comprehensive file management structure. Its friends call it AMDOS 8/8.

Those are the standard features. Hang on for the options.

System 8/8 speaks four languages fluently: BASIC, FORTRAN, COBOL AND PASCAL. Take your pick. (PASCAL is a new systems implementation language that lets you write more reliable software, lower your development costs and decrease software maintenance.)

We've also got in-circuit emulation, cartridge disks, 8085 and Z80 macroassemblers, CPU boards and a variety of data storage options.

If you want the best 16-bit CPU and the best development system in the business, call or write Advanced Micro Devices.

We've got what you want. No question about it.

Advanced Micro Devices

901 Thompson Place, Sunnyvale, CA 94086 Telephone: (408) 732-2400

Make reservations now for our 4-day seminar on the AmZ8000. Call (408) 732-2400, ext. 2325.

5th Annual IECI Conference Reviews Online Industrial and Control Microprocessor Applications

Although covering a large number of subject areas, the March 1979 conference of the IEEE's Industrial Electronic and Control Instrumentation Society concentrated on applications of microprocessors in process control and data acquisition. Other related subjects included energy, power, and distributed systems; consumer, automotive, and manufacturing control; diagnosis and testing; and biomedical. Evening panel sessions covered "8- and 16-bit Microprocessors" and "Software Development and High Level Languages." The following are summaries of some papers that related specifically to process control and data acquisition.

Microprocessor Systems Control Steel Mill Processes

Operation and maintenance of a new steelmaking basic oxygen plant (BOP) containing two 225-ton (202,500-kg) capacity furnaces and advanced pollution control equipment are controlled by two microprocessor systems.[1] One system controls conveyors that batch fluxes and additives; the other performs instrumentation and closed loop control. Many procedures conventionally regulated by analog instrumentation are now handled by microprocessor based control.

Kaiser Steel Corp's plant operates on a batch basis that optimally requires about 40 min/batch (a "heat"). Scrap metal and hot metal at about 2400 °F (1300 °C) are charged into the furnace. During the heat the furnace is enclosed by a charging door and a movable skirt, while a lance blows oxygen on the metal bath and various flux materials are added. Then the hot metal is poured into ladles for transfer to the next process.

Computer generated or operator specified requirements for fluxes or additives are met by the first system, in which five microprocessors control conveyors to batch material. Inputs are received from weight feeders and load cells on bins and transfer cars for both scrap and hot metals. All weights are transferred also to a management process computer for data logging.

In this system, one microprocessor controls hot metal, a second weighs scrap, a third handles flux batching, and a fourth processes batching. The fifth microprocessor controls communications among the various components, the process computer, and an operator's CRT display.

The second microprocessor system performs most of the instrumentation and closed loop control for lance oxygen, cooling water, and a closed hood suppressed combustion system with high energy scrubber for gas cleaning. It also troubleshoots problems within the equipment. A coaxial cable carries all data to the management process computer.

Eight analog control loops are handled by a single microprocessor. Each loop is programmed for the algorithm considered most suitable for current conditions, but can be reconfigured if process conditions change. Individual sensors are connected to the microprocessor system by two wires each, which also simplifies the addition or replacement of sensors.

The microprocessor based systems used in this installation are Honeywell TDC-2000 digital process control and data acquisition systems (see *Computer Design*, Jan 1976, pp 44-48). A basic module consists of a 16-bit microprocessor and factory programmed read only memory. Loop level modules link to an operator's console via a data highway. According to the presenter of this paper, "experience with hundreds of heats has shown that microprocessor control of industrial steelmaking is not only possible but effectively aids operators, maintenance people, and management personnel."

Microcomputer Eliminates Human Error In Nuclear Power Plant Reheat Temperature Control

Both temperature limits and the rate of temperature change of steam at the inlets of low pressure turbines in nuclear power plants must be controlled. In addition, thermal stresses and possible distortion of turbine stationary parts must be limited; the integrity of low pressure rotor discs must be protected; and the consequences of rapid temperature changes, large gradients, and temperature extremes must be minimized. Although these steps were previously carried out with pneumatic time pattern transmitters and electronic controls, a microprocessor based control system now eliminates most chances of human error.[2]

The reheat temperature controller system is made up of a Westinghouse Q-Line microcomputer card interfaced to I/O modules through a bidirectional, memory mapped I/O bus. The general purpose microcomputer card contains 512 bytes of RAM, 4k bytes of P/ROM, realtime clock, and serial communication port. A cable connection allows system expansion by connecting to other cards. Two 13-V supplies provide power. Signals are routed to and from the computer and digital input and output cards (see Fig 1) via the I/O bus.

(*Continued on p 72*)

Here's the fastest HP-IB* graphic peripheral available today... and it programs like a plotter.

With the HP 1350A Graphics Translator and one or more HP electrostatic CRT displays, there's no faster way of seeing your system's output. You can get a quick reading - then plot if hard copy is needed.

Because it's HP-IB* compatible, the 1350A is easy to add to your system. It lets you present different information simultaneously on up to four CRT displays.

And, it makes writing a program for a CRT display as easy as programming a plotter. An optional binary cassette tape for the HP 9825 Desktop Computer simplifies programming and lets you use the same routines on both CRT's and plotters.

The 1350A lets you update the display selectively. For example, in an application such as sequential testing, you can view multiple data plots (A) on a CRT and update only a portion of the display for rapid comparative measurements. It also provides convenient operator interaction. You can display program listings (B), normal and expanded displays, or a cursor and its coordinates.

Ideal for use with HP Data Acquisition and Network Analysis Systems, the 1350A Graphics Translator, priced at $3,450**, is a useful tool anywhere a fast, high-resolution graphic presentation of information is needed. Write for Application Note 271-1, or call your local HP field engineer for complete details.

*HP's implementation of IEEE Standard 488-1975
**Domestic U.S.A. price only

HEWLETT hp PACKARD

1507 Page Mill Road, Palo Alto, California 94304

For assistance call: Washington (301) 948-6370, Chicago (312) 255-9800, Atlanta (404) 955-1500, Los Angeles (213) 877-1282

068/12

CIRCLE 32 ON INQUIRY CARD

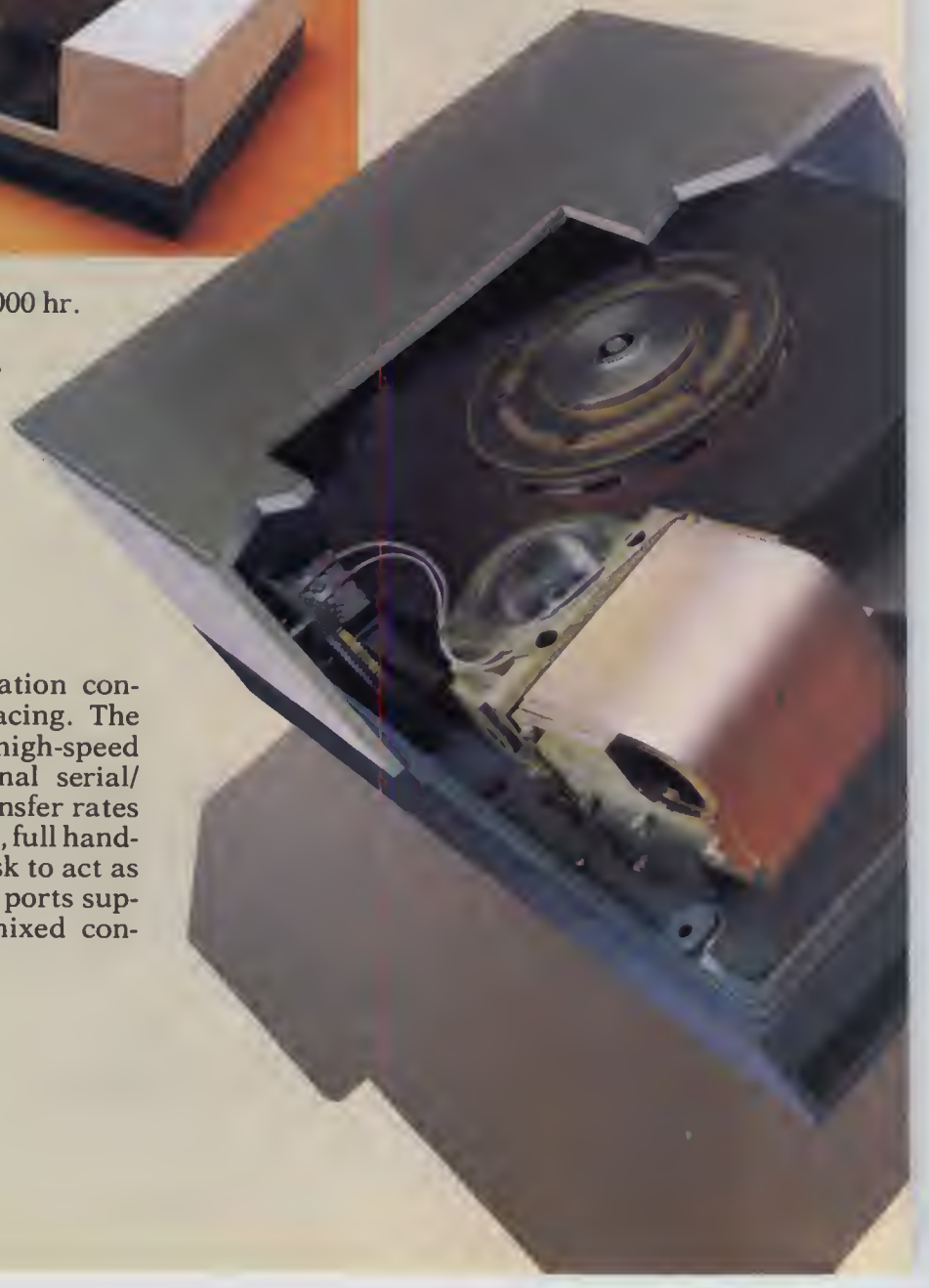
The intelligent disk architecture is available in STC

STC's new 2700 winchester disk family combines the intelligence of a microprocessor, 64k bytes of RAM, and a high-speed bus interface to offer you a versatile new disk architecture. An architecture that can help you achieve new dimensions in system speed and performance. Relieve CPU overhead burdens. Slash interfacing costs, and more.

Yet even without its advanced architecture, you'd still choose the 2700 disk family for its attractive price/performance and reliability values.

The 2700 family features formatted capacities of 39, 93, and 200 Mbytes, 25 msec average seek time, and OEM prices ranging from less than $3,600* (39 Mbyte) to less than $5,000* (200 Mbyte). With an 8000 hr. continuous operation MTBF, the 2700 will not just keep your customers happy, it'll keep your warranty expenses low.

*Domestic USA OEM prices in quantities of 100.



Powerful bus architecture for faster data rates and greater flexibility.

Gone are the speed and configuration constraints of serial, data-line interfacing. The 2700 disk family incorporates a high-speed byte-parallel interface, with internal serial/parallel conversion, to give you transfer rates up to 2 Mbytes/sec. The bidirectional, full handshake protocol permits any 2700 disk to act as master or slave, while built-in dual ports support radial, daisy chain or intermixed configurations.

Most important to you, the 2700 architecture offers maximum flexibility for applying these features. For instance, the architecture, coupled with the RAM buffer, permits continuous data transfer on both ports simultaneously. Thus your CPU can communicate with a 2700 on one port while disk-to-disk communication occurs on the other.

you'll need tomorrow Disks today.

The μP can unlock your system's hidden resources.

One way to boost your CPU's performance is to get it out from under system overhead and back to productive computing. The on-board intelligence of the 2700 gives you that capability. Routines such as drivers, data management and utilities can be offloaded to the microprocessor, freeing the CPU and bus for other tasks. But that's just the beginning.

For example, you can use the microprocessor to optimize throughput by means of zero millisecond writes and cacheing algorithms to speed read access.

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An intelligent controller in each drive. For free.

To help you get to the system level faster and easier, we placed 80% of the traditional controller functions within the 2700. Including all device dependent functions. Since you now only have to build a low-cost interface adapter—not a complete controller—your attachment costs are significantly reduced.

Low cost of ownership.

Fewer parts mean fewer failures. So the 2700 contains a minimum number of mechanical parts, only two of which move: spindle and actuator. The microprocessor contributes to this simplicity by replacing all sequencing and servo logic with firmware.

To eliminate scheduled maintenance, the 2700 dispenses with potentiometers. Dynamic adjustments are made internally under microprocessor control. And the 2700's closed loop air system means no filter changes.

If there's ever a failure, internal diagnostics isolate the problem to one of three subassemblies: logic board, head/disk assembly or power system. And these components uncouple quickly for fast repair. All of this translates into high MTBF, low MTTR, to reduce your warranty and field service costs.

To learn more...

about tomorrow's disk architecture, today, contact OEM Marketing, Storage Technology Corporation, P.O. Box 6, Louisville, Colorado 80027. Or phone (800) 525-2940; in Colorado 497-5151. In Canada: Ron Reardon, STC Ltd., 272 Galaxy Blvd., Rexdale/Toronto, Ontario M9W 5R8. Phone (416) 675-3350.

CIRCLE 33 ON INQUIRY CARD

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It can analyze voices, earthquakes, geological soundings and submarine signatures. It can recognize a sticky valve in an automobile engine or in a human heart.

There was a time when the phrase "FFT processor" conjured up the image of an entire bay of sophisticated electronic hardware, but that's all changed now.

Starting with just a single TDC 1010J, you can design your own FFT processor on a small pc card. It will operate on just a few Watts and the CPU's microcode need never even touch the data.

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Flexibility is a key feature of the TDC 1010J—it works on numbers as either two's complement or unsigned magnitude; the 35-bit accumulator can be directly pre-loaded, and you can round off the accumulated products to single precision.

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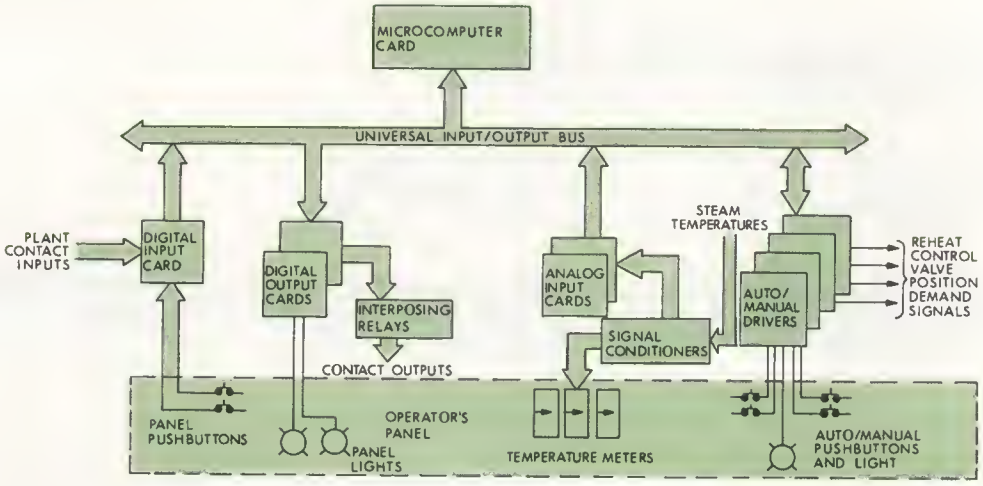

Fig 1 Nuclear power plant moisture separator-reheater controller configuration.[2] Byte oriented, bidirectional, memory mapped universal I/O bus provides CMOS interface between microcomputer and digital I/O cards and other system components

Physically the bus consists of printed circuit backplanes and flat cables to provide an uninterrupted, hardwired conductor for each signal or power line. Electrically it is a byte oriented CMOS interface with I/O cycles of 10 to 15 μs. Printed circuit cards can be mixed anywhere on the bus.

Because nuclear generated steam cannot be heated to extremely high temperatures, it contains a lot of moisture, which lowers overall efficiency. Therefore, a reheat temperature control procedure regulates steam bypassed to a separator-reheater where moisture is removed.

All I/O cards can be accessed by software via the bus and are periodically polled to obtain process information. Data are processed by software routines written in a high level FORTRAN type structured programming language called WEMAP. Software consists of a basic operating system and applications programs organized as shown in Fig 2.

The system is fully automated and requires no operator action except for selection and initiation of automatic modes through operator's panel pushbuttons. However, a manual mode allows the operator to bypass the microcomputer and position the reheat control valves directly.

Automatic procedures depend on the temperature at the low pressure inlet to each turbine. If thermocouples register a temperature greater than 300 °F (150 °C), a "hot" start is initiated by the computer. When steam flow through the turbine is adequate to ensure reliable temperature feedback, reheat control valves match steam to thermocouple temperatures and steam temperatures increase at a controlled ramp of 100 °F (38 °C)/h to a maximum of 425 °F (218 °C). When 35% turbine load is reached, the temperature ramp continues until full reheat is attained. On a "cold" start, the microcomputer opens and closes auxiliary valves at various turbine load points to initiate the temperature ramp at 35% load.

The microcomputer monitors steam thermocouples to be certain that the maximum high limit is not exceeded and that the mismatch does not go over 50 °F (10 °C). If either occurs, the condition is noted by status lights on the operator's panel and valves are repositioned to correct the condition.

Microcomputer Limits Torque for Propellers in Ship's Propulsion System

Controllable pitch propellers, combined with rapid response gas turbines, present propulsion control problems not encountered with steam or diesel plants. To overcome these problems, a torque computer was designed to compute engine torque and provide limiting signals to the ship's propulsion system.[3]

The microprocessor chosen for this application is an Intel 8085 with associated 8755 ROM and 8155 RAM because those three chips provide adequate program and data storage, five I/O ports, onchip clock, and simplicity of 5-V operation. Nearly all of the 2k of ROM are used for required program and tables, and almost all I/O lines are utilized by the interface circuits.

In the data acquisition procedure, four engine analog signals are converted to digital form by a micropro-

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Megastore goes where a disk drive used to go.

More to the point, Megastore keeps going long after a disk drive quits. Without motors, bearings, heads or platters, there's nothing to wear out, burn out or crash. No moving parts.

Megastore is the astonishing new fixed-head disk memory replacement from Ampex that uses reliable cores instead of rotating media. In the long run it saves a lot of money.

Megastore provides increased throughput, increased system availability, increased system uptime and reduced maintenance costs. A vastly better return on investment.

Unplug your disk and plug in Megastore. You'll get a half-million to four million bytes of capacity (in half-megabyte increments) that your existing software can't tell from the disk it was designed for. The only difference you'll see is a major improvement in throughput, because Megastore has a data access time that's anywhere from 1000 to 3000 times faster than the disk it replaces.

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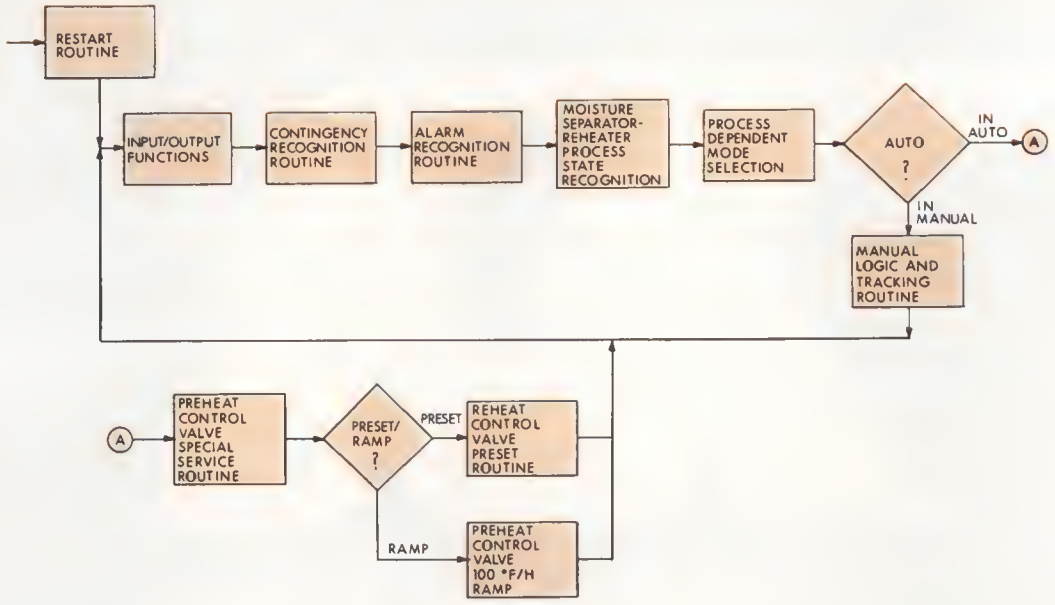


Fig 2 Organization of software programs for nuclear power plant steam reheat temperature control.[2] Applications programs run in continuous loop, scanning inputs and executing control strategies in same sequence every time. They are organized to avoid need for interrupts

cessor controlled DAC and comparators. Each analog input connects to a comparator. As a processor-generated voltage ramp increases, transitions at the comparator outputs signal the processor that an equality condition exists: the binary input to the DAC corresponds to the binary equivalent of an analog input.

Table lookup procedures are used to provide rapid computation. Tables corresponding to torque vs revolutions per minute for several values of engine pressure ratio were stored in ROM, and table lookup procedures combined with linear interpolation were used to calculate torque. After corrections for ambient pressure and temperature, binary values for torque and horsepower appear at the output ports and are converted to analog form. Specified accuracy of 3% was met or bettered.

Continuous Fabrication Machine Supervised and Automated

Because design of the control system for any large automated production machine must allow for requirements that cannot be defined at planning stages, flexibility must be included to meet changes. In the case of a 270 ft (82 m) continuous fabrication machine for producing reinforced insulation material to be used on liquid natural gas tankers, the practical solution was to choose distributed microcomputer hardware and modular software.[4]

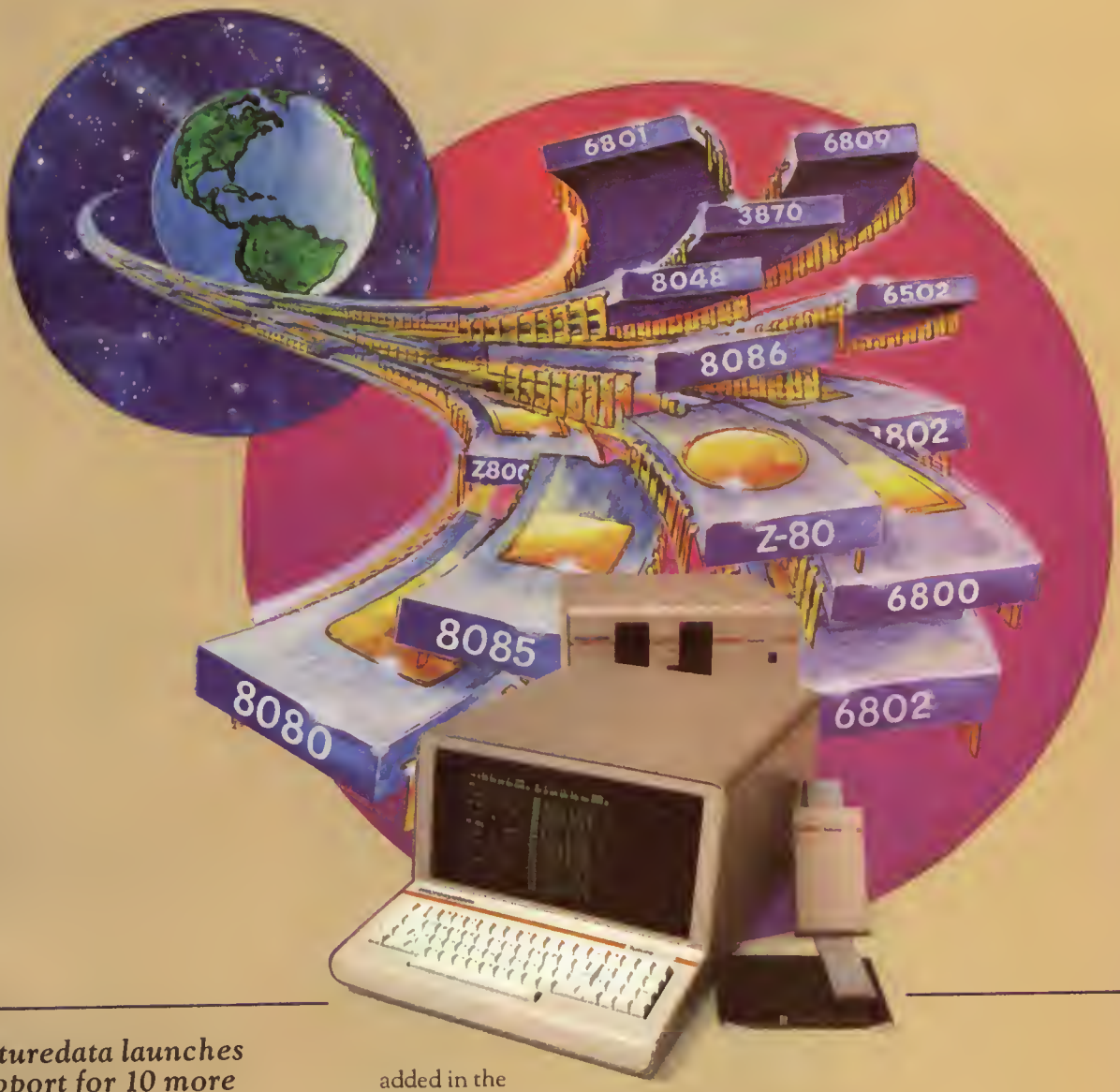
Initially, the machine winds yarn in two directions: crossways and longitudinally. Then a third-axis filament is inserted. Foam is poured into the mold just before the web enters a pressure chamber. As the insulation leaves the chamber (in the form of a continuous log of rigid reinforced foam), it is cut into lengths by a programmable flying crosscut saw.

A basic microcomputer in this control system is made up of two circuit boards: one contains CPU, system clock, RS-232 interface for a terminal, I/O lines, RAM, and EPROM for program storage; the other contains more I/O interface and EPROMs plus communications bus interface circuits. The combined boards provide 48 inputs, 55 outputs, and 4k bytes of program memory. By adding another of the second type of board, capacity can be increased to 80 inputs, 87 outputs, and 6k bytes of program memory. The present multiprocessor system uses 357 inputs, 291 outputs, and 50k bytes of memory. About half of the inputs can be programmed as interrupt signals.

A synchronous serial data bus that provides communications among the several microcomputers terminates through differential line drivers and line receivers at each computer. An adapter provides serial to parallel or parallel to serial conversion for interfacing with the CPU data bus. One pair of wires carries serial data while another handles the 5-kHz synchronizing clock.

Task level software packages, each a combination of standardized software modules and task dependent modules, are designed to operate independently. Firmware containing the task software is in the task com-

How to put μP with the mad, mad world of product development.



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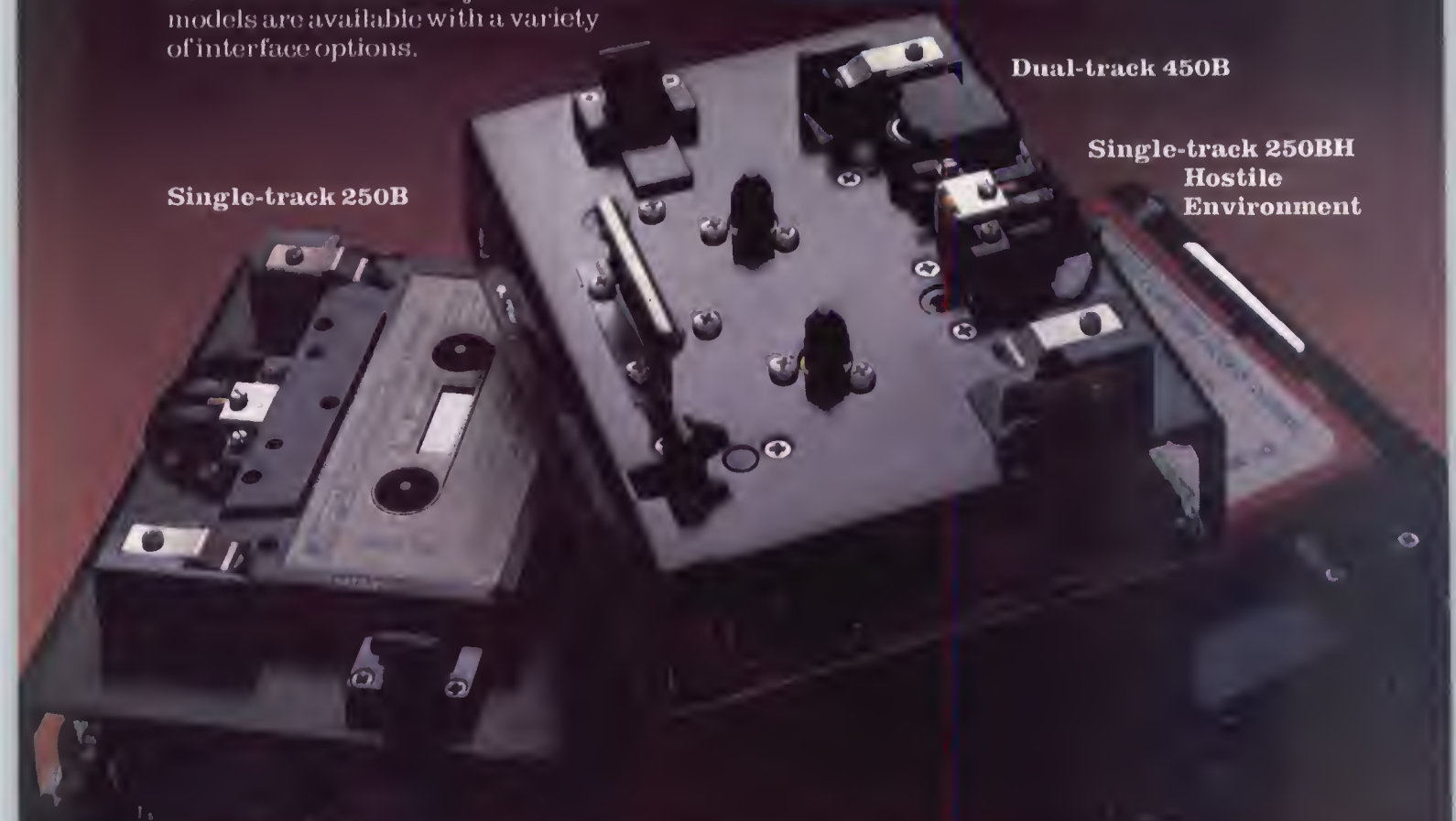


Dual-track 450B

Single-track 250BH Hostile Environment

Single-track 250B

CIRCLE 37 ON INQUIRY CARD

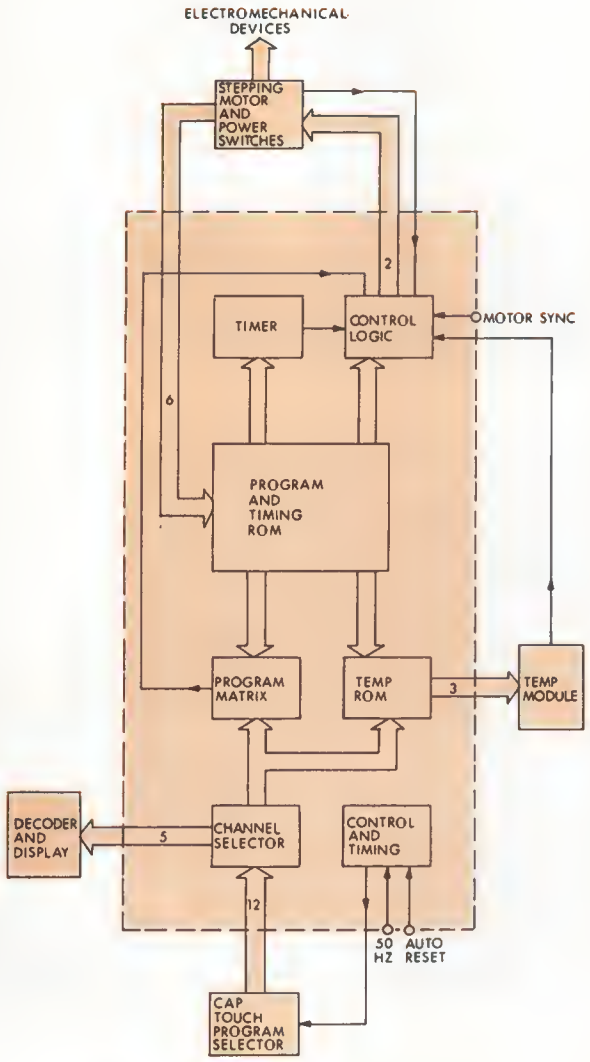


Fig 3 System architecture for washing machine CMOS controller.[5] Logic is simplified by having up to 64 program steps arranged sequentially, with specific time value assigned to each

puter. When power is turned on, each task computer begins carrying out its program regardless of the other systems.

The total supervisor software package is made up of independent program modules, each to be executed in a fixed amount of time: 27 ms when all modules are online, but greater with fewer modules so that total execution time is constant and overall system timing is not affected. An executive routine in the supervisor determines if a program module is to be run, in what sequence, and for how many time periods.

An automatic sequencing mode is used for all production operations. Once the machine is started, the operator should have nothing to do until the machine is to be shut off. The only exception would be if a major problem occurs. Notification of that condition is provided by a printout at a computer terminal that enables operator interaction.

The computers constantly check performance of mechanical devices and sensors in the facility. Fault isolation is provided as a printed message for the operator.

CMOS Unit Controls Washing Machines

Washing machines and other similar appliances such as dishwashers and tumbler dryers are now being manufactured with CMOS ROM programmable controllers that use line frequency as the clock.[5] If the power supply fails, all signals on the chip disappear and data are retained by holding the voltage on the chip with a capacitor.

Main functions of the controller are capacitive touch input circuit logic, program and timing ROM, timer, and control logic for a stepping motor that drives the power switches (Fig 3). Power switching is performed by a 64-position motor-operated rotary disc. The disc pattern determines the sequence and timing of switch openings and closings.

A capacitive touch panel has 10 program inputs, 1 economy modifier input, 1 erase input, and a 7-segment LED display that identifies program number. Because a touch must be maintained for 80 ms before the system accepts a valid signal, there is immunity from electrical interference. In addition, the system will not accept a signal if more than one input is touched.

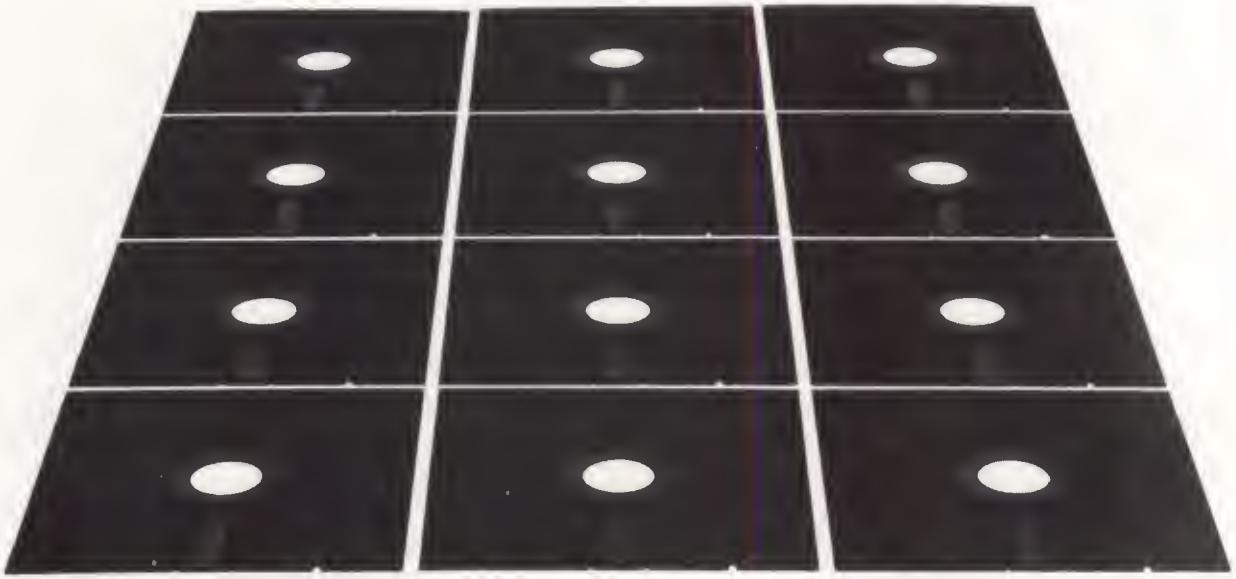
SCADA Systems Maintained at Electric Power Production Plants

Supervisory control and data acquisition (SCADA) systems have evolved over the years at Pennsylvania Power & Light Co from one-on-one master-remote multiplexing systems, with each remote having a dedicated master, to master station electronics under control of a mainframe computer, and now to replacement of hardwired dedicated logic devices by microprocessors. One such recent application uses a microprocessor to implement a communications controller that interfaces the mainframe computer to serial telephone communications lines.[6]

Although Fig 4 shows only one portion of the system, information can be gathered from several remote stations through use of multiple controllers operated asynchronously under computer control. The communications controller (Fig 5) performs all parallel to serial and serial to parallel conversions, message formatting and buffering, error detection, handshaking control, and communications line switching.

Major functional areas of controller hardware are main computer interface, line buffer, and communication line interface. The main computer interface enables high speed parallel data exchange between mainframe computer and microprocessor line buffer. (Because the

O.L.D.



The Mini-Wini is the new 8" fixed disk that stores 20 megabytes.

That's right 20 (count them) megabytes. The same 20 megabytes you'd have to string more than 12 floppy disks together to get. We thought it was about time somebody offered the reliability and efficiency of a fixed disk in a smaller size, at a smaller price. So here it is. We call it the Mini-Wini. Otherwise known as our D8000 fixed disk.

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When we say the same size, we mean the same size. That means you can upgrade your storage capacity easily. All you have to do is buy the Mini-Wini. Of course, some controller redesign will be required.

The Mini-Wini saves you money.

It's the lowest-cost way to get 20 megabytes in an 8" floppy envelope. With it, you can expand the on-line capacity and value of your present desk-top system without having to redesign the chassis you now have.

The point is, the Mini-Wini allows you to put out a better product without spending a lot of money. It also allows your customers to save money. Why hassle with stacks of floppies or large old-fashioned disk drives, when one small fixed disk will do?

Mini-Wini is a trademark of Pertec Computer Corporation.

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The Mini-Wini offers ease of interface.

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It's made by Pertec Computer Corporation. Which is reassuring. We not only have the capabilities to produce innovative new products, we also have the production capacity to supply them when we say we will. So if you want the Mini-Wini, check with us.

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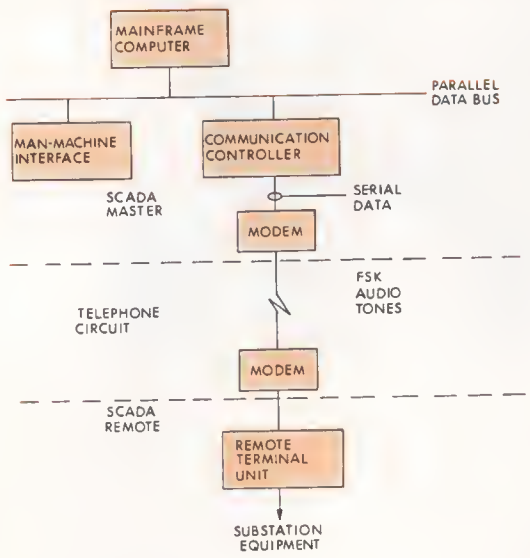


Fig 4 Key elements of part of PP&L SCADA system.[6] Several such system segments operate under control of mainframe computer. Microprocessor based design replaces hardwired dedicated logic

selected microprocessor was inadequate for the overall application, many interface functions are handled by dedicated hardware.)

Line buffer hardware is based on a Motorola 6800 microprocessor with programmable interface adapter for I/O, a programmable timer module for generating bit time intervals, 1k bytes of scratchboard RAM, 2k bytes of program EPROM, and associated logic ICs. The communication line interface includes serial data I/O, request to send, and carrier detect lines plus other lines to control analog switches that select communications lines.

Line buffer software operates at four priority levels. The most time-critical logic is executed at high interrupt priority in the shortest possible time; lower priority functions are less time-critical. All serial data transfers to and from remote terminal units are handled by nonmaskable interrupt processing; all parallel data transfers to and from the main computer are handled by interrupt request processing. Reset interrupt processing performs hardware and software initialization.

Ground level processing utilizes a software priority structure in which an ordered list of request flags is continually scanned. Routines are initiated by interrupt service routines through the request flags. When a flag is set, the loop scan is interrupted by jumping to the required logic; when the logic concludes, request list scanning resumes at the top of the list.

PP&L found that replacing hardwired logic controllers with single-board microprocessor based communication controllers reduced costs by half. Currently, production communications controllers are being installed at each of six SCADA master stations.

SCADA System Applied to Multimicroprocessor Electric Power Installation

Multimicroprocessor configurations in electric power generation supervisory control and data acquisition systems eliminate many of the disadvantages of conventional SCADA systems.[7] In particular, they provide

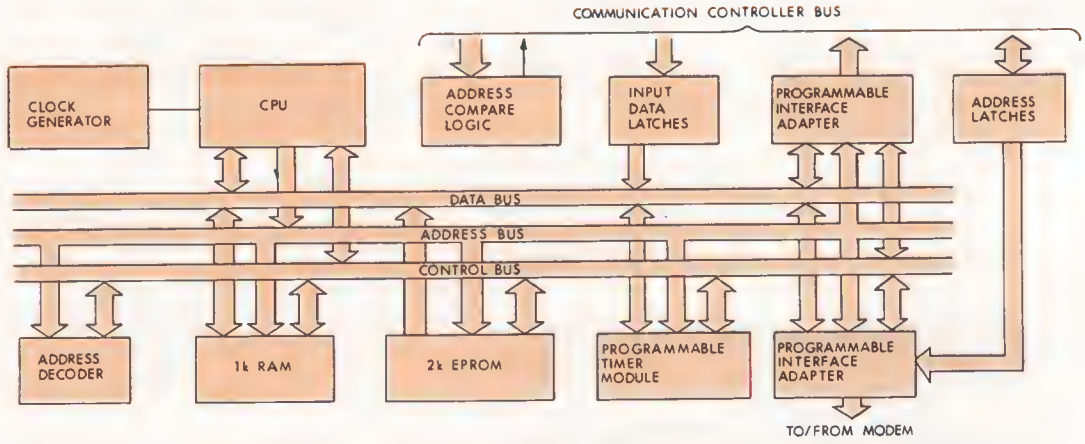
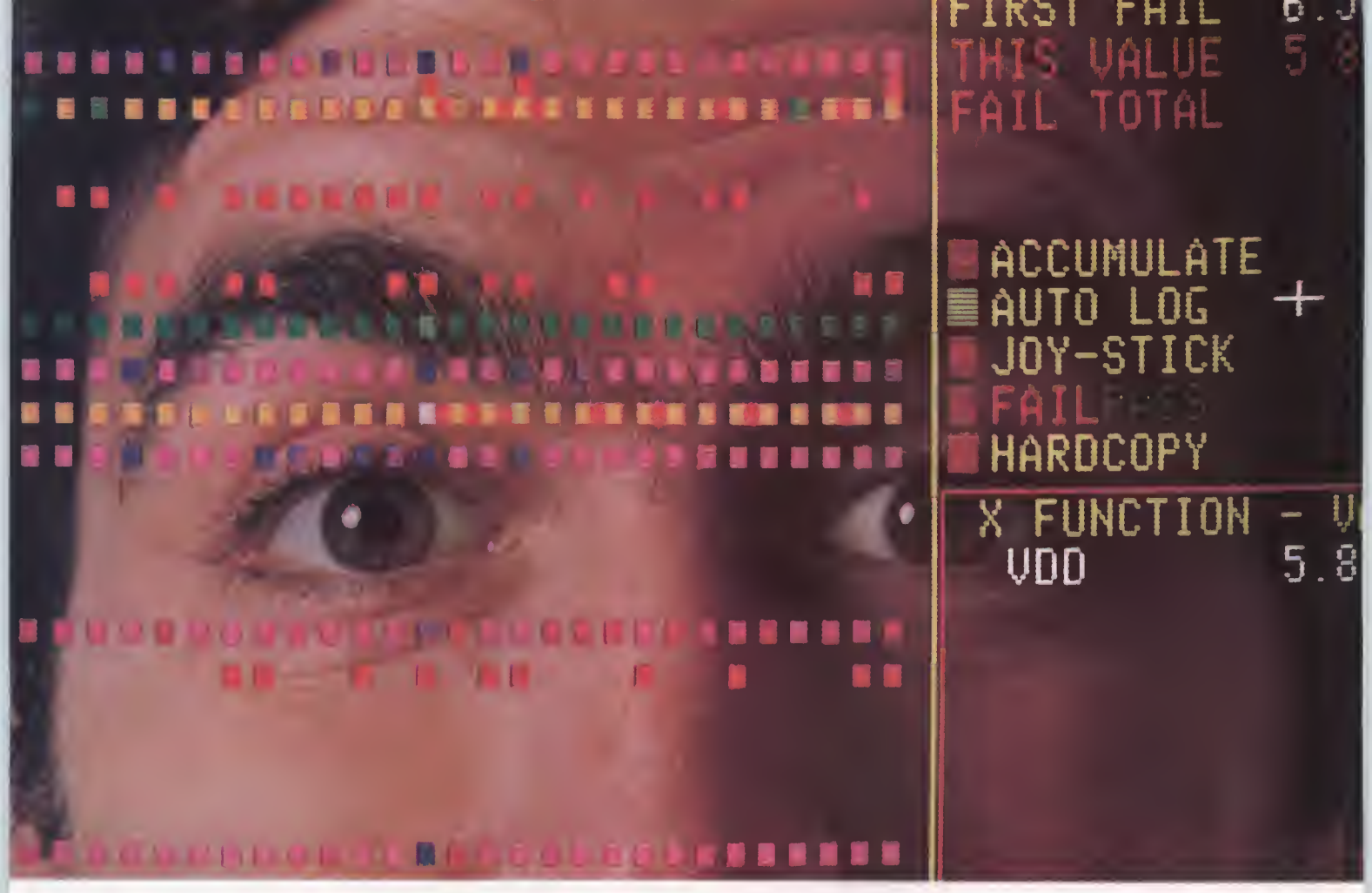


Fig 5 SCADA system communication controller hardware.[6] Multiple controllers communicate with mainframe computer over address/data/control bus structure



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Better 4k statics. New 16k and 64k dynamics.

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Today, more and more memory users are learning their way around the new devices with the help of the Teradyne J387, equipped with Real-Time Bit Mapping.

With RTBM you get all the way inside a memory, watching bits fail under changing test conditions on RTBM's 19-inch full-color display. It's a view of device behavior you just can't get anywhere else.

Shorter device design times.

With the J387's interactive programming, characterizing new devices is a breeze. The system asks questions and the design engineer answers them in the appropriate device language.

Using either software programming or a joy stick, the engineer can control timing edges, voltage levels, and test patterns. He can then see, bit by bit, how the memory is affected, with different colors clearly indicating different bit fail conditions.

Characterization time for new devices is dramatically shortened. So you can introduce new designs faster and with greater confidence.

Moreover, RTBM gets the right individual—the design engineer—completely into the characterization process.

Duplicate actual operating conditions.

The best way to see if a device checks out is to check it out under the specific operating conditions for each application. RTBM has the speed and the capacity to do just that.

Memory users can totally qualify incoming devices, as well as the vendors who supply them.

Further down the line, this means a substantial savings. Because end-product reliability goes up while rework time to correct faults goes down.

The total system.

Teradyne's J387 has a lot going for it besides RTBM.

There's a Test System Administrator that integrates information from multiple systems. And a Data RAM that permits testing of RAMs, ROMs or PROMs in any mix you wish. And Automatic Edge Control that saves hours of calibration time and countless human mistakes.

It's all part of the definite edge Teradyne's J387 can give you. Send for our free brochure. Write: Memory Product Group, Teradyne, 21255 Califa Street, Woodland Hills, CA 91367.

CIRCLE 39 ON INQUIRY CARD

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We'll also tell you which approach will best meet the unique requirements of your application. Such factors as encoded or non-encoded, number of keys, lighted positions...and more. This is particularly important since keyboard applications vary so greatly in complexity and use that there really isn't any one style of keyboard or one technology that's best for all.

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CONTROL
SHIFT
ESC
TAB
SHIFT LOCK
SHIFT
BREAK
CLEAR
ON LINE
CTRL
SP
CR
RETURN

versatility for system modifications, are easier to implement, remove the problems of larger computers, are reliable, and are relatively inexpensive.

A typical multimicroprocessor SCADA system includes 10 to 50 remote stations for each master. Each remote station selects and controls 100 points, has 150 status signals, and measures 150 values. Data are transmitted in direct memory access mode at speeds of 200, 600, and 1200 baud.

In this system, an asynchronous bus operation was initiated because the bus controller is simpler (no master clock required), control can be readily bypassed if a malfunction occurs, each node can operate independently, and software is less complicated. However, other problems appeared: processing time had to be increased, and partial hardware or software malfunction could cause failure of the entire system.

To eliminate these problems, a simple operating system was developed that achieves high response times in a realtime environment. Except for bus data control, function programs are executed on an interrupt-enable mode. Each functional unit is connected to dual system buses through interfaces with buffer memory, enabling each microprocessor unit to perform operations at the same time.

References

All of the following items are included in the *IECI '79 Conference Proceedings.*

1. D. L. Browne, "Microprocessor Control for Industrial Steelmaking BOP Shop," pp 29-31
2. F. Behringer and J. Bukowski, "Microprocessor Controls for Turbine Reheat Steam Temperature," pp 32-36
3. C. J. Rubis *et al*, "A Microprocessor Torque Computer for Gas Turbines," pp 37-40
4. D. F. Baker *et al*, "A Distributed Multiprocessor Control System for a Continuous Fabrication Process," pp 142-145
5. B. Ketelaars and P. Tharma, "A Universal CMOS Controller for Washing Machines," pp 202-207
6. D. E. Woods, "A Microprocessor Based SCADA Communications Controller," pp 58-61
7. S. Ryusawa *et al*, "Multi-Microprocessor Applied SCADA System for Electric Power Systems," pp 68-72

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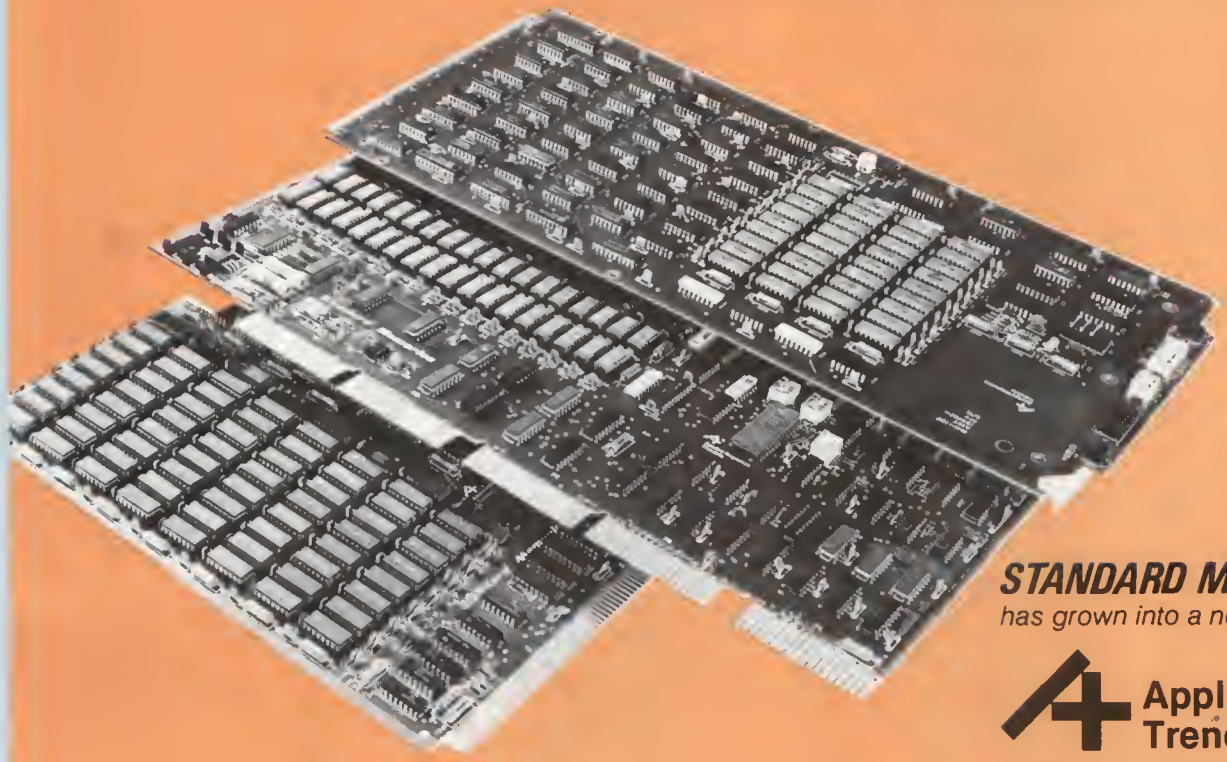

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Low Cost Acquisition and Control System Fits Small System Application

LN540, a low cost computer based realtime data acquisition and control system offered by Leeds & Northrup, North Wales, PA 19454, for small scope electric utility applications, is organized around a CP40 multifunction control processor with up to 64k of solid state memory including battery backup, a color CRT terminal with graphics capability, a floppy disc for program storage, and a printer for alarm and periodic logs. A communications network control subsystem handles all communications with as many as 1500 data points through a family of Conitel remotes. A color CRT terminal provides an interface for all phases of system operation.

Software includes basic supervisory control and data acquisition programs with a conversational compiler to accommodate expansion, a display generator, and a comprehensive set of diagnostics. All programs are stored on diskettes.

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Data Acquisition System Provides Online Test Results

Because it supplies test results on essentially a real-time basis, the digital engineering online (DE-OL) terminal is claimed to meet the requirements for a number of industrial/manufacturing test applications. An integral data acquisition subsystem digitizes analog signals from a variety of types of sensors for input to the system's microprocessor, and an 8-channel differential input multiplexer can be interfaced to existing chart recorders or load cell amplifiers.

A tape cassette for data logging, backup batteries to protect memory during a power failure, and BASIC language programming for the user who prefers to write dedicated analysis programs are options on this terminal offered by Alewife Systems Corp, 127 Alewife Brook Pkwy, Cambridge, MA 02138. A programmed software package is provided that automatically tests for a broad range of factors. In addition, a 4-station variation permits one microprocessor to monitor four testers simultaneously, printing out the data as soon as they become available.

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Multiple-Axis Control Capability Added to CNC Unit

Hardware/software features added to versions of the Bandit CNC positioning control, offered by Summit/Dana Industrial, PO Box 1906, Bozeman, MT 59715, now provide capabilities not on standard units: lathe control and six axes of machine tool control. Available in both open and closed loop configurations, standard units include 250-command memory, operator switchable inch/metric operation, and user selectable resolutions of 0.001 and 0.0001″ or 0.01 and 0.001 mm.

Standard programming features provide subroutines, repeated operations, feed rate control, programmed dwell, 3-axis control, memory image I/O capability, insert/delete program editing, and random tool selection with automatic tool changers. Firmware/hardware options include 999-command memory, linear and circular contouring, I/O in EIA or ASCII code, online external program storage and retrieval, absolute programming, programmable canned cycles, autocycles, and autoroutines.

Specifically tailored hardware and software permit the control to be used in lathe operations. The user can mix radius and diameter dimensions in any desired sequence, with resolution of 0.00005″ (0.00127 mm) along the radial axis and automatic routines for threading pullout, and turning and facing. In this application, the Y axis in the conventional 3-axis mill unit is replaced with a U axis, used for radius entries. The X axis is used for diameter entries.

A turning and facing routine permits the user to program the lathe control for the final part path in a subroutine that is then used to work up to the final dimension in a multiple pass cycle. This allows the rough and finish cuts to be generated from the same block of instructions.

Added firmware enables the CNC, formerly limited to three axes, to handle up to six axes of motion, including two rotary. The controller can be programmed to operate a given axis in the primary mode, the secondary mode, or the slaved mode, in which the primary and secondary axes move in unison. Tool offsets are applied independently to each primary and secondary axis, even if they are slaved.

By closing a DIP switch inside the CNC, the user can cause the secondary X and Y axes to be regarded as rotary axes. The user has his choice of 0.001° or 0.01° resolution with rotary axes.

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COMPARING ARCHITECTURES OF THREE 16-BIT MICROPROCESSORS

Increased power and flexibility of 16-bit microprocessors, previously available only in minicomputers, can make the designer's decision process complex. Although a direct comparison of the 9900, Z8000, and 8086 is somewhat difficult, register and addressing techniques warrant evaluation

Henry A. Davis American Microsystems, Inc, Santa Clara, California

As 16-bit microprocessors become readily available, applications incorporating them will increase tremendously. In systems where greater processing power and reduced size are important, these single-chip microprocessors will replace both board level minicomputers and smaller word size microprocessors. Applications likely to incorporate 16-bit microprocessors are diverse but are alike in that they have typically reached the limits of 8-bit microprocessors. As prices drop, capability loaded, low cost equipment will begin to incorporate 16-bit microprocessors simply to provide a competitive edge. These microprocessors offer speed, expansion, and generally easier software implementation. As a result, many designers who are only recently familiar with 8-bit microprocessors will have to learn to evaluate and design with 16-bit devices.

Memory

The AMI- and TI-9900, Intel 8086, and Zilog Z8000—three 16-bit microprocessors*—all have extended addressing capabilities; in addition, the 8086 and the Z8000 possess onchip paging and segmenting. Using an offset address scheme, the 8086 can address up to 1M bytes; using a similar segmented addressing method, the Z8000 can address up to 48M bytes; and using externally paged memory, the 9900 can address up to 16M bytes. Note that these schemes essentially bring the rudiments of memory management on board the microprocessing unit (MPU) and use existing discrete solutions to address requirements.

Memory addressing does not limit the usefulness of any of these three MPUs, however. Since few systems address as much as 64k bytes, address capabilities will probably not be a large factor in selecting one chip over another. Few applications programs except compilers and interpreters use more than 16k bytes. Extended addressing will only be a factor in a system replacing high end minicomputers. In these applications, memory and peripheral interfacing are responsible for the major share of system cost.

Speed

Another widely publicized capability of 16-bit MPUs is clock speed. The published speed of the 9900 is 3.3 MHz, the target speed of the 8086 is 5 MHz, and

*This article is restricted in coverage to the architectural design considerations, in general, and the register structure and addressing modes, in particular, of three selected single-chip 16-bit microprocessors. It is recognized that additional 16-bit microprocessors are commercially available and operational.

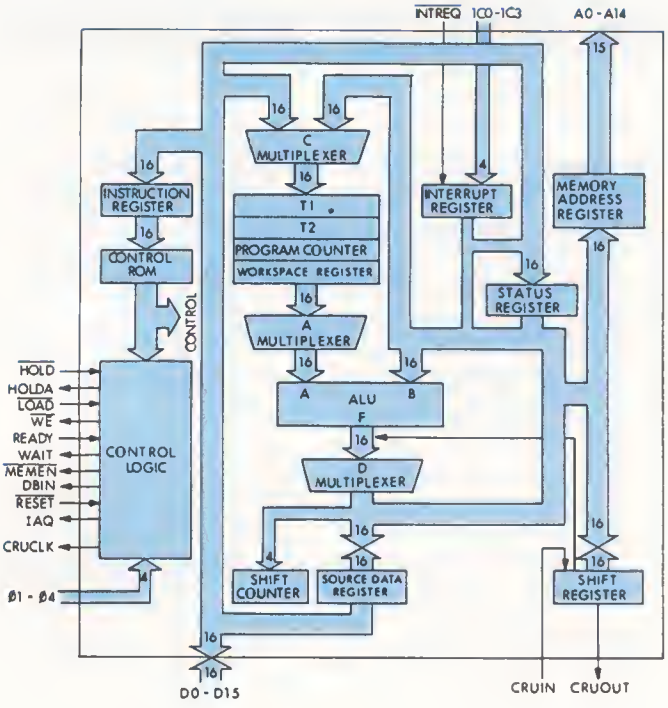


Fig 1 9900 functional block diagram. Architecture reveals absence of programmable registers and I/O port interface logic and presence of significant interrupt handling and serial-to-parallel data conversion logic. Only three registers are programmable—program counter (PC), status register (SR), and workspace register (WR). Separate nonmultiplexed data and address buses can operate at speeds up to 4 MHz but require 4-phase clock

the Z8000's speed is 4 MHz. Clock speeds reveal little about instruction execution times and are not necessarily a measure of throughput; therefore, they influence performance only as a basis for determining cycle times and, thus, execution time. For example, the 9900 multiply instruction is faster than the corresponding 8086 instruction, yet the 9900 clock speed is slower. System throughput will probably not significantly differ among the three MPUs, but costs for support chips and memory will differ dramatically. Ultimately, fitness of a particular MPU is an application dependent constraint.

Miscellaneous Design Considerations

During system design, other factors demand consideration equal to or greater than that given to clock speed. Project design turnaround time—which directly affects price and deliverability—is accomplished more quickly by availability of software support, ease of system hardware and software development, and system component count.

Design evaluations are best treated through investigating different MPU architectures, instruction sets, software tools, capabilities, throughput, memory addressing, and minimum system parts. The three 16-bit MPUs can be separated into two general architectural groups: memory oriented machines (the 9900) and accumulator based machines (the Z8000 and 8086).

9900 Architecture

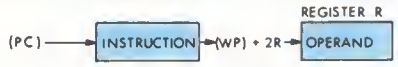
The 9900 architecture is designed as a downward compatible device from a minicomputer (Fig 1); the basic instruction unit is a 16-bit word with bit, byte, and word capabilities. Downward compatible capabilities include providing complex instructions in a single word and then permitting simple adaptation of the instruction to one of eight addressing modes (Fig 2). Each addressing mode specifies either program/data or input/output (I/O) space. Consequently, by selecting one of 69 available instructions and an addressing mode, a programmer has an effective work set of 483 instructions. Second and third words can be added for immediate operands and extended address capabilities. Two-address (memory-to-memory), single-address, and no-address (immediate) instruction formats are furnished.

To round out the instruction set, 16 extended operations (XOPs) are left undefined. These operations are executed in software, are somewhat slower than the basic instruction set, and offer additional flexibility for system design and software implementation.

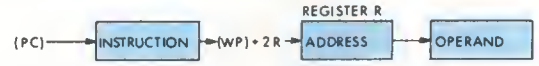
Register Organization

The 9900 utilizes a memory-to-memory architecture that provides workspaces of 16 registers in memory for each level of interrupt or subroutine. Memory-to-

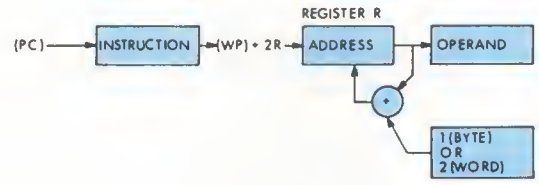
WORKSPACE REGISTER ADDRESSING (R): REGISTER R CONTAINS OPERAND VALUE USED BY INSTRUCTION



WORKSPACE REGISTER INDIRECT ADDRESSING (*R): REGISTER R CONTAINS ADDRESS OF OPERAND

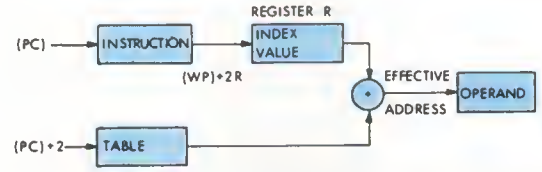


WORKSPACE REGISTER INDIRECT AUTO INCREMENT ADDRESSING (*R+): REGISTER R CONTAINS ADDRESS OF OPERAND. AFTER ACQUIRING OPERAND, CONTENTS OF REGISTER R ARE INCREMENTED BY 1 IF BYTE INSTRUCTION AND BY 2 IF WORD INSTRUCTION



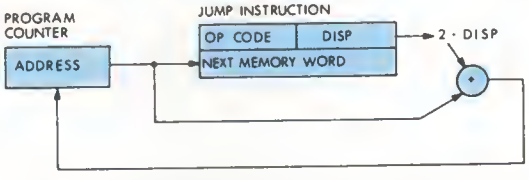
SYMBOLIC (DIRECT) ADDRESSING (@ LABEL): WORD FOLLOWING INSTRUCTION CONTAINS ADDRESS OF OPERAND. THIS IS ABSOLUTE ADDRESS WITH RANGE OF 0 TO 65k BYTES

INDEXED ADDRESSING [@ TABLE (R)]: WORD FOLLOWING INSTRUCTION CONTAINS BASE ADDRESS. REGISTER R CONTAINS INDEX VALUE. SUM OF BASE ADDRESS AND INDEX VALUE RESULTS IN EFFECTIVE ADDRESS OF OPERAND



IMMEDIATE ADDRESSING: WORD FOLLOWING INSTRUCTION CONTAINS OPERAND. ONLY WORD VALUES MAY BE USED WITH THIS ADDRESSING MODE

PROGRAM COUNTER RELATIVE ADDRESSING: LAST EIGHT BITS OF INSTRUCTION CONTAIN 2's COMPLEMENT OFFSET VALUE. 8-BIT SIGNED DISPLACEMENT IN RIGHT BYTE (BITS 8 THROUGH 15) OF INSTRUCTION IS MULTIPLIED BY 2 AND ADDED TO UPDATED CONTENTS OF PROGRAM COUNTER. RESULT IS PLACED IN PC



CRU RELATIVE ADDRESSING: RIGHT BYTE OF INSTRUCTION CONTAINS 2's COMPLEMENT OFFSET VALUE. 8-BIT SIGNED DISPLACEMENT IN RIGHT BYTE OF INSTRUCTION IS ADDED TO CRU BASE ADDRESS (BITS 3 THROUGH 14 OF REGISTER 12). RESULT IS CRU ADDRESS OF SELECTED CRU BIT

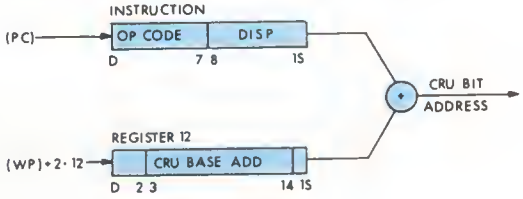


Fig 2 9900 addressing modes. Eight modes are available for addressing random memory data (eg, program parameters and flags) or formatted memory data (eg, character strings and data lists). Derivation of effective address for each addressing mode is depicted

memory architecture is normally found in much larger mainframe central processing units (CPUs), where context switches (subroutine calls or interrupts) are numerous and must be handled at high speed.

The workspace register (WR) concept is particularly valuable for applications requiring frequent servicing of interrupts and context switching. In more conventional register-to-register architectures, a context switch requires storing and reloading all or part of the contents of the register field, at a cost of one memory reference for each store or fetch.

The workspace register system exchanges the contents of the program counter (PC), workspace pointer, and status register (SR), so that the 9900 can accomplish a complete switch in one instruction (three stores and one load). Containing powerful programming capabilities, the workspace register identifies the first of sixteen 16-bit memory locations that act as 16 general purpose registers in read/write memory rather than in the CPU. Similar time saving occurs on return to the original routine. However, design tradeoffs apply, and the workspace concept is no exception. Increased programming flexibility associated with context switching is accompanied by slower register access times because the registers are in main memory as opposed to residing on the CPU chip.

The 9900 is not intrinsically a stack oriented machine. Instead, a stack of workspaces may be created. Because the architecture is somewhat nonorthogonal, handling stacks and stack pointers requires one extra instruction for one of the complementary stack operations because there is no auto decrement addressing mode.

Interrupts

The 9900 provides up to 16 levels of interrupt, 15 of which are available to the designer. The highest priority level is reserved for the reset function, all others are available to external devices, and each level can be shared among several devices. Interrupt occurs at the end of a currently executing instruction. The MPU fetches the new context workspace and program counter, the interrupt vector locations, and stores the previous WP, PC, and SR contents in register locations 13, 14, and 15, respectively, of the new workspace.

To establish priority, the interrupt mask level decrements to one less than the level of interrupt being serviced at the time. Program linkage is preserved in the event of a higher priority interrupt since the processor automatically inhibits interrupts until after execution of the first instruction of the service routine. The result is simpler programming and more efficient handling of external interrupts. Each process handled has a "clean" CPU, following interrupt servicing, and 16 new registers in memory. A programmer does not have to take into account the status of each register in order to avoid clobbering it with the results of the new routine.

CRU Capability

A unique capability of the 9900 is the direct command driven communications register unit (CRU). The CRU requires as little as two low cost 16-pin transistor-transistor logic (TTL) chips to interface with 16 external I/O devices, and supplies up to 4096 directly addressable bits each of input and output. I/O bits can be addressed individually or in fields of 1 to 16 bits. The 9900 employs three dedicated I/O pins: CRUIN (CRU data in), CRUOUT (CRU data out), and CRUCLK (CRU clock), as well as 12 bits (A3 to A14) of the address bus to interface with the CRU system. The low pin count of CRU interfacing and CRU based peripherals is highly advantageous in many applications. When the system can tolerate small amounts of overhead associated with this serial/parallel device, as in switch sampling or universal asynchronous receiver/transmitter—universal synchronous/asynchronous receiver/transmitter communications, system cost is lowered by the ability to use low cost TTL components.

Z8000 General Architecture

The Z8000 is a register or multi-accumulator oriented machine that provides sixteen general purpose 16-bit registers (Fig 3). With one exception (register 0), no registers are implied in an instruction and none have special restrictions. Bottlenecks such as dedicated accumulators are therefore avoided and programming is efficient and straightforward. The Z8000 is stack oriented and utilizes both system and normal stacks. Up to 48M bytes of memory can be directly addressed, and instructions to manipulate data types that range from bits to long words (32 bits) are included.

Segmentation

Two versions of the Z8000 are offered—the Z8001 48-pin segmented CPU and the Z8002 40-pin nonsegmented CPU. The Z8002 uses 16-bit addresses that can be manipulated as words, as in the 9900. For low performance applications, this version can directly address 64k bytes of memory in each of its eight addressing modes (Fig 4). Two of the eight modes (base address and base indexed) apply only when the full address space is available. The Z8001 provides direct addressing in applications requiring larger amounts of memory. For medium performance applications, a segmented Z8001, together with a Z8010 memory management unit, allows direct access to 4M bytes of address space, and for high performance, a Z8001 and multiple pairs of Z8010s permit use of several 8M-byte address spaces. These 23-bit addresses are split into two parts: a 7-bit segment number points to the beginning of a contiguous area within the address space, called a segment, and a 16-bit offset addresses any location relative to the beginning of the segment. The two parts of the segmented address must be manipulated separately. The Z8001 can be used in either a segmented or nonsegmented mode.

To provide segment relocatability, a process of address translation is performed by a separate Z8010 memory management unit external to the Z8001. This unit converts segmented addresses—also called logical addresses—to physical addresses. Transparent to the software, this mapping is a traditional method of memory management, similar to that used in the Digital Equipment Corp PDP-11.

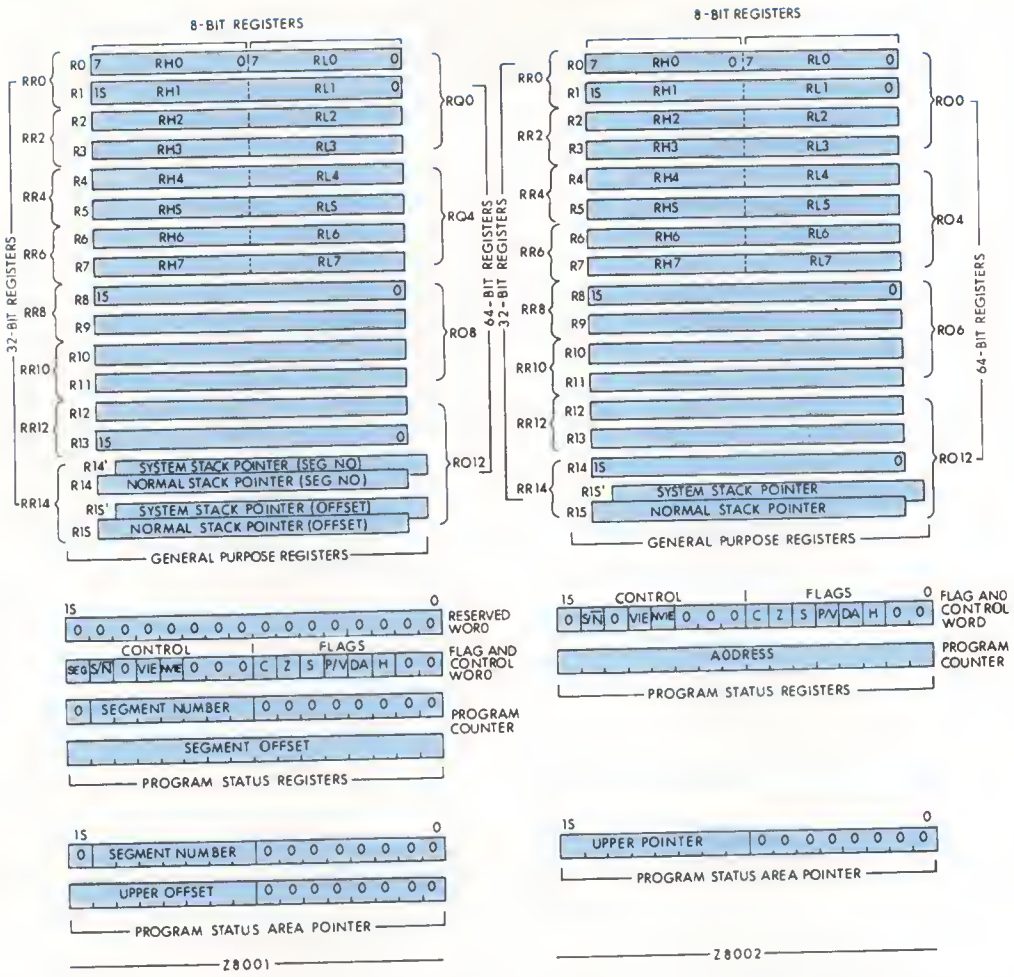


Fig 3 Z8000 register organization. CPU offers sixteen 16-bit general purpose registers and set of special program status registers. All general purpose registers can be used as accumulators, and all but one as index registers or memory pointers. Register flexibility is created by grouping and overlapping multiple registers

Instruction formats and addressing modes exhibit some differences between the nonsegmented Z8002 and the segmented Z8001. In the nonsegmented Z8002, R15 contains the implied 16-bit stack pointer; in the segmented Z8001, RR14 contains the 32-bit segmented stack pointer (R14), the 7-bit segment number, and R15, the 16-bit offset value. Because the stack pointer is part of the general purpose register set, all instructions may be used to operate on it in conjunction with memory locations and constants.

Two modes of operation provided in the Z8000 are system and normal. One copy of the stack pointer is for system mode and the other for normal mode. Although the stacks are separated, it is possible to access the normal stack registers while in the system mode by using the load into (or from) control register (LDCTL) instruction. This process protects the operating systems.

Refresh Principles

Perhaps the most unique capability of the Z8000 is a 16-bit counter that automatically refreshes dynamic memory. The counter contains a 9-bit row counter, a 6-bit rate counter, and a single enable bit (bit 15). A special refresh memory access is made at programmable intervals. The 9-bit refresh row counter is incremented by two, each time a prescaler times out, allowing up to 256 rows for future high density memories; present 16k dynamic random access memories have 128 rows.

A programmable 6-bit modulo-n counter (n = 1 to 64) determines the time between successive refreshes. With a 4-MHz clock, the refresh period is programmable from 1 to 64 μs. The prescaler is freerunning, but refresh access can be delayed up to one refresh interval without missing a refresh. Refresh can be totally dis-

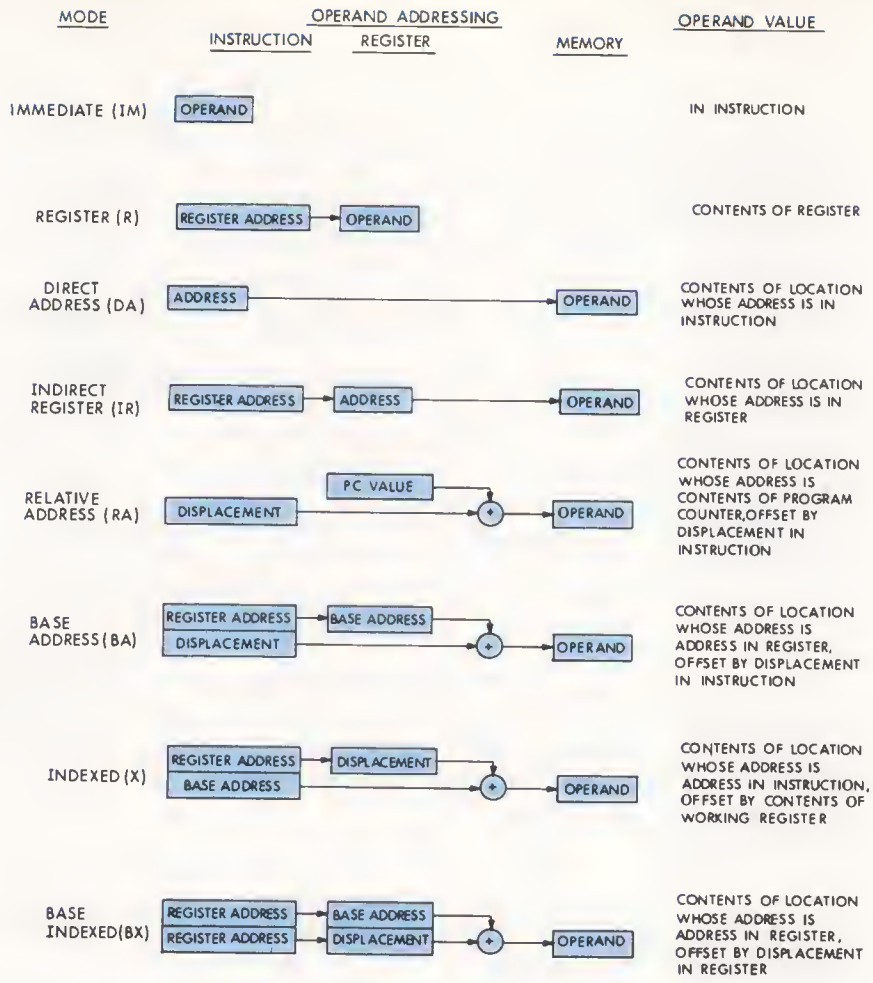
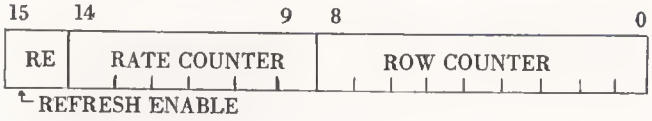


Fig 4 Z8000 addressing modes. Information included in Z8000 instructions consists of function to be performed, type and size of data elements to be manipulated, and location of data elements. Locations are designated by register addresses, memory addresses, or I/O addresses. Each of eight addressing modes defines address space it references and method used to compute address itself. Addressing modes are explicitly specified or implied by instruction

abled, if necessary, by programming the enable bit. The Z8000 refresh counter is set up as



8086 Architecture

Spawned from the family architecture of 4004, 8008, and 8080 microprocessors, the 8086 provides an increase in processing power over its predecessors (Fig 5). Designed to be generally upward compatible with the 8080, the 8086 is a natural step up for designers currently utilizing 8-bit microprocessors. By remaining mostly software compatible with the 8080, the 8086 holds the promise of relatively easy software portability.

Upward compatibility with the 8080/8085 is maintained by pairing the 8080 registers (BH, BL, CH, CL, DH, DL) to define four 8086 16-bit registers (Fig 6). Each half of these four registers is independently accessible with much the same instruction set available in the 8080. Additionally, the pairs can be accessed to perform 16-bit arithmetic. Seven new registers have been added to handle the expanded architecture, including the source index (SI) and destination index (DI), for easy data movement. The base pointer (BP) allows flexible accessing of scalars and arrays by continuing the beginning address of a data structure. The effective address may be computed in a variety of ways including base plus displacement and base plus displacement plus index. Additional flag bits are included to handle the expanded arithmetic capabilities.

To accommodate both 8-bit and 16-bit devices, the 8086 uses a 20-line address bus and a 16-line data bus with lower order 16 address bus lines time multiplexed with the data bus. To support either minimum or maximum mode flexibility, several pins perform dual system functions based on MN/$\overline{\text{MX}}$ connections.

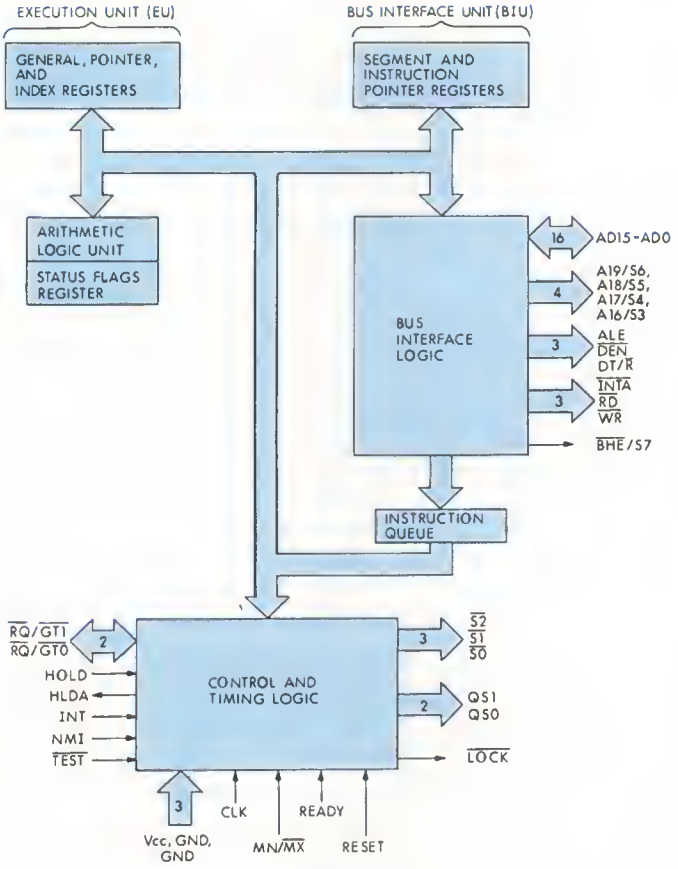


Fig 5 8086 CPU functional block diagram. Internal functions are partitioned into two processing units—bus interface unit (BIU) and execution unit (EU). These units can interact directly, but mostly perform as separate asynchronous operational processors. BIU provides functions related to instruction fetching and queuing, operand fetch and store, and address relocation; this unit also furnishes basic bus control. EU receives prefetched instructions from BIU queue and provides unrelocated operand addresses to BIU. Memory operands are passed through BIU for processing by EU, which then passes results to BIU for storage

Four segment registers handle memory management onchip by memory space division. This division of program and data space allows the programmer to break away from classical architectures for formulating reentrant code. The actual address—called the physical address—is formed by adding a 4-bit effective address to a 16-bit segment register, resulting in a 20-bit address. Each segment is 64k bytes in length, allowing up to 256k bytes to be addressed at any one time as combined code, stack, and data. Assignment of segment space is left to the designer, but for practical systems, the code segment usually begins at $FFFFF_{16}$ to handle the reset vector.

The segmented memory implementation map is under explicit program, rather than hardware, control. If a program is 70k bytes long, simply allowing the instruction pointer to increment will cause the program to "jump" to its beginning. To get to the extra 5k of program, the code segment register (CS) must be suitably changed. This may be accomplished by a compiler/loader package that would insert the necessary code. The programmer must maintain the extra four bits of the address; it is never explicit in operand addressing.

In a similar manner, data are accessed by adding contents of the offset or data segment (DS) register to the operand address. Again, the DS is explicitly under programmer control and is not automatically incremented/decremented by the hardware. Extra segment (ES) and stack segment (SS) registers are likewise controlled. Such schemes are often implemented in mainframe computers for extended addressing, and the method is well understood by designers.

Interrupts and Interfacing

There are 256 interrupts for the 8086, 1 nonmaskable and 255 maskable. The nonmaskable interrupt (NMI) causes the flags to be pushed onto the stack and makes an indirect call to a subroutine through transfer vector element two (address 8_{16}). Intended for catastrophic

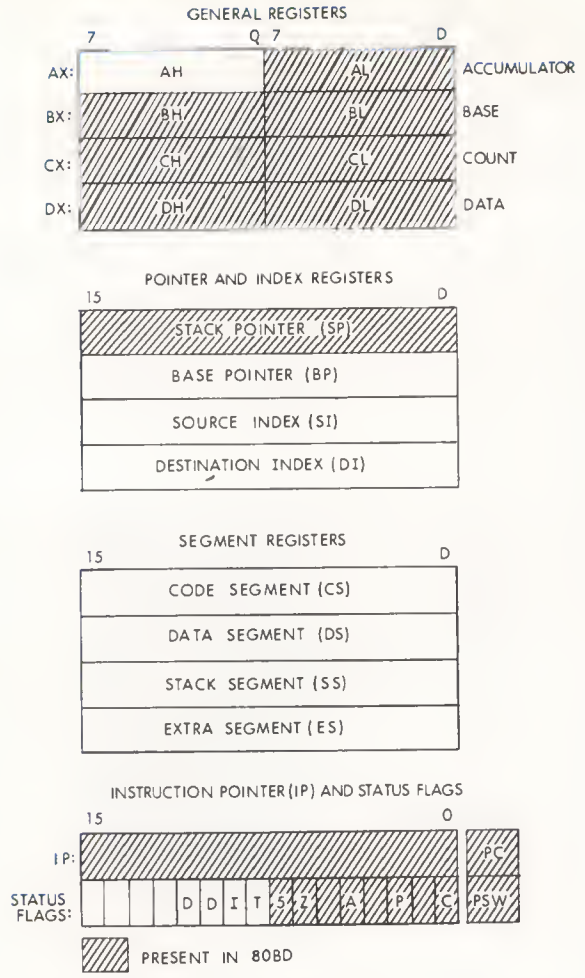


Fig 6 8086 register organization. Register structure of 8086 has seven more registers and four more flags than 8080. Major difference is that extra registers can process 16-bit data. However, general registers remain 8-bit byte addressable

systems failure, the NMI may corrupt a critical code sequence, such as initializing SS and SP, and it must be used with caution. Four bytes are needed to indicate the offset and segment addresses for each vector element.

For the 255 maskable interrupts, upon receipt of an interrupt request, the MPU issues two interrupt acknowledge signals; the interrupt interface must respond with an interrupt number on the second signal. Then, the 8086 pushes the flags and performs an indirect transfer through the appropriate transfer element.

Hardware and software compatibility requires that interrupts 0 to 31 be reserved for the manufacturer's exclusive use. Five interrupts are currently defined for internally generated interrupts: divide by zero, single step, nonmaskable interrupt, 1-byte interrupt instruction, and interrupt on overflow. These interrupts have absolute top priority, followed by nonmaskable interrupts. Because of the register structure, handling interrupts will usually mean pushing all registers onto the stack upon entering an interrupt subroutine and popping the value in preparation to exit the subroutine.

General Processor Comparison

Accounting for major architectural differences between microprocessors (ie, memory-to-memory vs accumulator based) is nearly impossible since most evaluation procedures rely on instruction mixes or particular algorithms. Performance evaluations usually use KIPS (thousands of instructions per second) as a means of comparison. Several methods of determining KIPS include instruction mixes, program kernels, synthetic jobs, and benchmarks.

Instruction mixes are based on the frequency of use of each instruction in a computer. In order for this method to be valid, all computers involved are the classical single-instruction stream, single-data stream, or single-address type (accumulator based SISD). This constraint prohibits an "intrinsically fair" method of comparison since the 9900 is a different machine type. Instruction mixes are usually developed on a base CPU and then applied to other target CPUs. Many different instruction mixes can be developed which characterize different applications. Evaluations using these mixes that involve different architectures simply are neither accurate nor representative.

The remaining methods of evaluation (kernels, synthetics, and benchmarks) require that each CPU under evaluation be programmed. They are, in general, more difficult and costly to apply but yield more accurate results. In particular, it may be possible to account for architectural differences between the various microprocessors. Unfortunately, the results are highly dependent on the programmer's basic skills, algorithm choice for each microprocessor, and expertise with each of the CPUs.

A kernel is the most frequently executed portion of a complete program. In order to apply the kernel technique, the complete program must be designed. The resulting kernel may be a floating point routine or a character translation. The difficulty is that different CPUs may lend themselves to different algorithms. Thus, each kernel may require several different algorithms and test programs.

Benchmarks are actual subroutines of a complete package while a synthetic job is an artificial program which is representative of an actual benchmark. Both are often written in a high level language, but introduce another variable: the efficiency of the compiled code. In particular, programs in a high level language test the code generating facilities of the compiler in addition to the CPU capabilities.

Direct Evaluation

First step in evaluating a 16-bit microprocessor is to draw some generalizations, such as memory requirements, for the application. Second, identify the class of problem that needs a solution. Tasks which involve a multiply and accumulate, like digital filtering, may fit on the 9900 best—if it is a major kernel. On the other hand, register intensive programs may fare better

TABLE 1

Microprocessor Parameter Comparison[1]

Parameter	9900	Z8000	8086
Address Bus	15 bits	16/23 bits	20 bits
Clock Frequency (min/max)	0.5/4.17 MHz	8 MHz	0.5/5.0 MHz
Clock Phases/Voltage Swing	4/12 V; 1/TTL	1/TTL	1/TTL
Data Word	16 bits	16 bits	16 bits
Dedicated I/O Lines	3	0	0
Direct Address	32,768 words	8M bytes/64k bytes	1,048,576 bytes
Instruction Word	1 to 3 words	2 to 6 bytes	1 to 6 bytes
Longest Instruction/Time	divide/31 μs	divide/90 μs	16-bit signed integer division/ 37.8 μs
Number of Basic Instructions	69	>110	97
Package Type	64-pin DIP	40- or 48-pin DIP	40-pin DIP
Power Requirements	5 V at 50 mA −5 V at 0.1 mA 12 V at 25 mA	5 V at 300 mA	5 V at 275 mA
Shortest Instruction/Time	Branch/2 μs	Many/750 ns	Many/400 ns
Derived Data Based on Clock Frequency:			
Clock Frequency	3.3 MHz	4 MHz	5 MHz
Divide (16-Bit)	37.2 μs (worst case) 27.6 μs (typ)	N/A	33 μs
Memory-to-Memory Add (16-Bit)	9.0 μs	N/A	N/A
Move Byte (Word)	4.2 μs	N/A	4.6 μs
Multiply (16-Bit)	15.6 μs	17.5 μs	26 μs
Register-to-Register Add (16-Bit)	4.2 μs	2.25 μs	600 μs
Variable Shift	6 μs + 0.6 μs*L[2]	N/A	4 μs + 0.8 μs*L[2]

[1]Partial comparison of 16-bit MPUs demonstretes relative strengths and weaknesses. For example, 9900 performs well in memory-to-memory functions, while 8086 and Z8000 possess major attributes in register oriented algorithms. Data imply that each microprocessor type demands design attention to both the application and the algorithms.

[2]L stands for the number of positions of shift.

on the 8086 or Z8000 (Table 1). Third, program a kernel for each microprocessor using an appropriate algorithm. Lastly, do not solve problems that do not exist. If speed is not important, consider instead price, availability, and capital investment as a basis for choice. Including subjective analysis in the decision, contrary to opinion, makes sense; the entire design team must agree with the choice.

A strict one-on-one analysis cannot be made as a generalization when considering these three 16-bit microprocessors. Programming time is substantially the same among all three. Code for the 8086 and Z8000 is typically within a few percent, while the 9900 may require a few extra instructions to make up for some nonorthogonality. Speed of execution is algorithm dependent. The different architectures lend themselves to different programming techniques.

Bytes of memory used are almost identical between the 8086 and Z8000. The multiple address architecture of the 9900 may require some extra memory for equivalent code. Because access times are faster for the 8086 and Z8000 than the 9900, memory costs will tend to be higher for these microprocessors. Where speed is not an important factor in interfacing, the 9900 CRU can lower systems cost by using 9901 or standard 7400 TTL.

Other observations are that the 8086 and Z8000 allow upward portability from the 8080 and Z80, respectively, while the 9900 is upward compatible with several minicomputers. Long-term direction is an important factor here. High level languages exist for the 9900; similar languages for the 8086 and Z8000 will follow soon.

Table 2 indicates that all three microprocessors have similar capabilities with the possible exception of execution speed. Actual speed comparisons must be made on the basis of representative kernels or benchmarks; instruction mixes may be misleading due to the radical architectural differences. Minimum system package count varies among the three MPUs; however, as the size of memory gets larger, the 9900 parts count advantage will diminish.

Each of the three microprocessors has its own set of attributes and limitations. The 9900 has its principal use as an applications solution for dedicated systems. Maturity of the hardware and software, along with low parts count, are major factors in choosing the 9900 for a dedicated system. Additionally, the memory-to-memory architecture and efficient interrupt structure are pluses in its choice. However, using the 9900 in a large (greater than 64k-byte) memory system requires additional hardware for memory management.

TABLE 2

Microprocessor Instruction Comparison*

	9900	Z8000	8086
Add Register-to-Register (Reg)	✓	✓	✓
Add Register-to-Memory (Mem)	✓	✓	✓
Add Mem-Mem	✓	N/A	N/A
Add Byte	✓	✓	✓
Absolute Value	✓	N/A	N/A
Add Immediate	✓	✓	✓
Clear Register	✓	✓	Programmed
Clear Memory	✓	✓	Programmed
Divide, 16-Bit Unsigned	✓	✓	✓
Divide, 16-Bit Signed	N/A	✓	✓
Load Immediate	✓	✓	✓
Move Mem-Mem	✓	✓	✓
Move Byte Mem-Mem	✓	✓	✓
Multiply, 16-Bit Unsigned	✓	✓	✓
Multiply, 16-Bit Signed	N/A	✓	✓
Shift Variable	✓	✓	✓
Programmed I/O	8k bits	64k bytes	64k bytes
Vectored Interrupts	16	256	256
Priority Interrupts	16	256 (uses external)	256 (uses external)
Address Space	64k bytes	48M bytes	4M bytes
Compare Word	✓	✓	✓
Compare Byte	✓	✓	✓
Decimal Adjust	N/A	✓	✓
Increment/Decrement	✓	✓	✓
Multiprocessor Control	N/A	Semaphores	Semaphores

*All three microprocessors have similar software capabilities with a few exceptions. The 8086 and Z8000 have increased addressing space, I/O space, and add the instructions used in COBOL type applications—decimal adjust. Additionally, these microprocessors include multiprocessor lockout functions based on semaphores. Effectivity of multiple microprocessors does not increase linearly. For two linked microprocessors, the effective power is 1.7, and for three linked microprocessors the effective power is 2.2.

The relative newness of the Z8000 and 8086 has braked their implementation. Extended addressing capability and enhanced instruction sets aim these microprocessors at the mid-range minicomputer market. The large number of interrupts also favor large systems. The combined hardware and software feature sets of these two microprocessors make them advantageous for operating systems and compiler operations. When used in the proper applications area, all three microprocessors can be both cost effective and technically valid.

Acknowledgement

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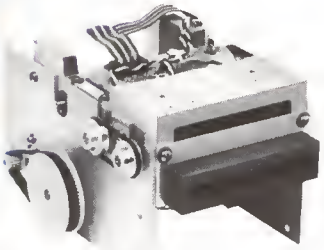

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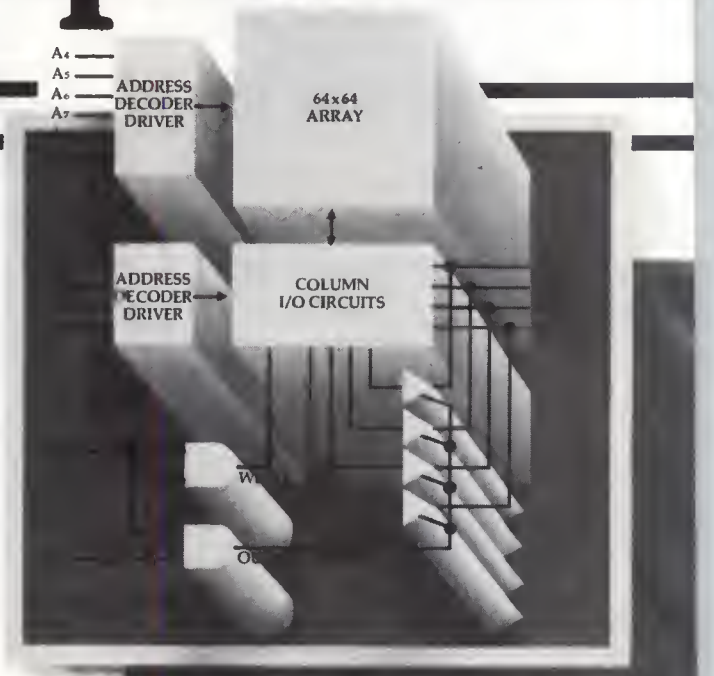

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PRACTICAL HARDWARE SOLUTIONS FOR 2's COMPLEMENT ARITHMETIC PROBLEMS

Difficulties encountered in designing format conversion, addition overflow, and magnitude comparison functions into 2's complement arithmetic hardware are resolved by workable hardware designs based on standard ICs

Thinh V. Nguyen ITT General Controls, Glendale, California

Hardware implementations of 2's complement number systems, particularly in digital signal processing, continue to increase. This popularity stems from (a) the single representation of number 0, as compared to the −0 and +0 representations necessary in a signed magnitude or signed 1's complement system; (b) straightforward subtraction since actual subtraction is not required (the subtrahend is first inverted and then added, with a carry equal to 1, to the minuend, and the addition always ignores the resulting carry); and (c) algorithms available for multiplication include Booth's and modified Booth's, and large scale integrated multipliers are available for handling large bit sizes (24 x 24) at high speed (200 ns). Despite established methods, however, 2's complement hardware implementation presents design problems in practice, particularly in high speed applications that may require millions of arithmetic operations per second.

In signal processing, arithmetic operations basically consist of multiplication, addition, and comparison. Although current technology allows the construction of ultra high speed processors, this approach requires a custom made chip and is usually expensive. A common design practice is to use standard integrated circuits (ICs) because of the convenience in interfacing to various components, low power consumption, and normal off-the-shelf availability. However, digital design of 2's complement number arithmetic processors using standard ICs [transistor-transistor logic (TTL) and low power Schottky TTL (LS/TTL)] presents difficulties. Conversion of number formats, overflow in addition, and magnitude comparison for signed 2's complement are the three most commonly encountered problems.

Conversion of Number Formats

Signed magnitude, signed 1's complement, and signed 2's complement are the most common in binary representation number systems. In some applications, however, binary numbers appear in different formats rather than the same format throughout due to system constraints. For example, data from an analog to digital converter often are signed magnitude, whereas multipliers use 2's complement. Another example is a magnitude comparison using a standard comparator (7485) that requires data to be delivered in signed magnitude format. These inconsistencies in binary number representations within the same hardware unit require a number converter to perform format conversion wherever needed.

Signed 2's Complement To/From Signed Magnitude Conversion

To convert a signed magnitude binary number to

signed 2's complement, the following rule applies: for a positive number (sign bit is 0), signed magnitude and signed 2's complement are the same; for a negative number (sign bit is 1), first invert the number and then add a binary 1. Exactly the same operation is performed to convert signed 2's complement to signed magnitude. For example, in an 8-bit field

$+103_{10}$	= 0 1100111	Signed magnitude and signed 2's complement
	↑ Sign bit	
-103_{10}	= 1 1100111	Signed magnitude, negative
	↑ Sign bit	
	= 1 0011001	Negative 2's complement
	↑ Sign bit	
	1 1100111	Negative magnitude
	1 0011000	Invert
	+ 1	Add one
	1 0011001	Negative 2's complement
	↑ Sign bit	

To convert 10011001 (negative 2's complement) back to negative magnitude, perform the same operation: invert, then add 1.

1 0011001	Negative 2's complement
1 1100110	Invert
+ 1	Add one
1 1100111	Negative magnitude
↑ Sign bit	

Conversion hardware implementation is straightforward with an inverter and an adder (Fig 1). This circuit utilizes medium speed 4-bit adders (74283) with ripple carry implementation, in which the carry from the less significant 4-bit adder propagates to the next significant 4-bit adder. In applications where speed is critical (eg, a digital filter that requires thousands of such additions per second), propagation delay in the adders may be a problem, especially when the word size is large (16 bits or more). It is, of course, feasible to employ a high speed arithmetic unit (74181) and a lookahead carry generator (74182), but these parts would increase cost and complexity.

To overcome propagation delay, an improved adder circuit (Fig 2) always adds a 1 to each individual adder; however, their outputs are chosen by data selectors, depending on whether the less significant adder stage produces a carry or not. Since each adder operates independently, instead of propagating the carry bit from one to another, total add time is equal to that of one adder plus the delay due to one data selector. For example, assuming that LS/TTL ICs are used, a 16-bit addition using this scheme has a total add time of T = 15 ns (for adder) + 9 ns (for data selector) = 24 ns, compared with 45 ns for the scheme of Fig 1.

For a larger number of bits (greater than 16), the time saving may be significant because total add time is always 24 ns, no matter how many bits are involved. The only disadvantage of this circuit is that additional hardware (74LS157) is required, which may impose cost and physical constraints in some applications.

Signed 1's Complement To/From Signed 2's Complement Conversion

Because the forward and reverse conversions involved in changing from signed 1's complement to or from signed 2's complement representations do not follow the same procedure, two individual examples are presented.

1's complement to 2's complement—A positive binary number requires no conversion procedure. A negative binary number requires that 1 be added to the 1's complement number; this addition can be configured as discussed previously, ie, in conjunction with the data selectors (74LS157). For example, in an 8-bit field where the 8th bit is the sign bit

$+103_{10}$	= 0 1100111	Signed magnitude and signed 2's complement
	= 0 1100111	Positive 1's complement
	= 0 1100111	Positive 2's complement
	↑ Sign bit	
-103_{10}	= 1 1100111	Signed magnitude, negative
	= 1 0011000	Negative 1's complement
	+ 1	Add one
	= 1 0011001	Negative 2's complement
	↑ Sign bit	

The circuit that implements this example comprises two parallel 4-bit adders (74LS283) and a data selector (74LS157). The sign bit determines if addition with 1 is required. For a positive binary number, addition with 0 leaves the number unchanged; for a negative binary number, addition with 1 converts to negative 2's complement.

2's complement to 1's complement—For a positive binary number no conversion is necessary. For a negative binary number three steps must be executed: invert, add 1, and invert again.

-103_{10}	= 1 0011001	Negative 2's complement
	1100110	Invert
	+ 1	Add 1
	1100111	
	1 0011000	Invert again, negative 1's complement
	↑ Sign bit	

An 8-bit conversion circuit followed by two data selectors (74LS157) can perform the 2's complement to 1's complement conversion whether the binary number is positive or negative. For positive numbers, no conversion is required because the representation is the same in both formats. Therefore, for asynchronous operation, in which a step starts as soon as the previous step is finished, the conversion can be skipped and data can be passed directly through two data selectors. The sign bit is used to switch the data to output. For a negative binary number, the data selector routes the number back to the conversion circuit. However, in

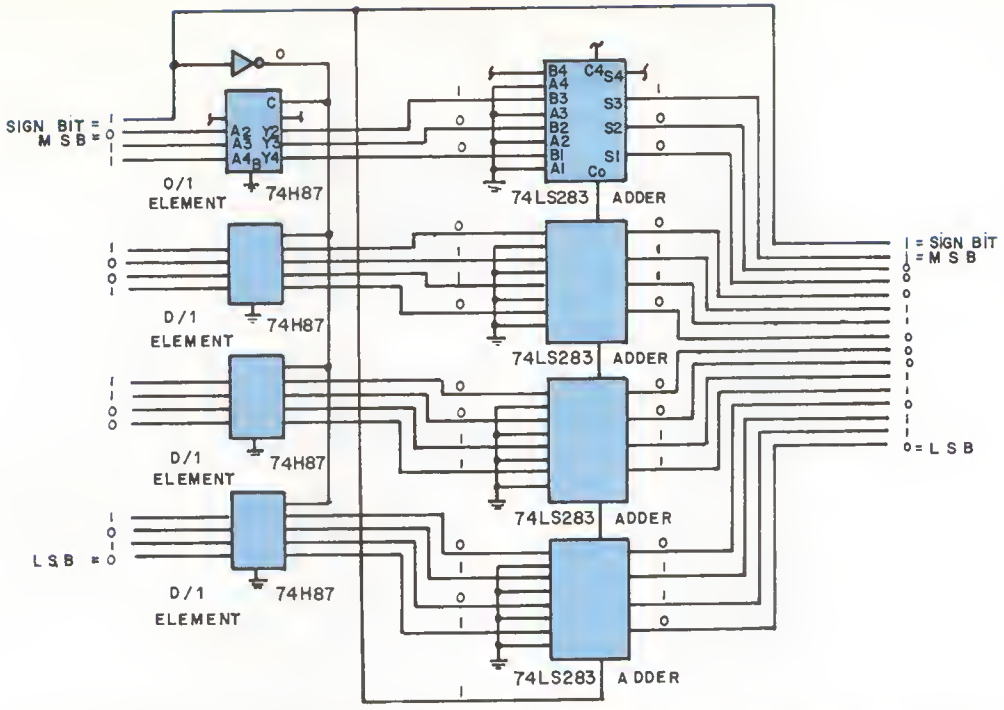

Fig 1 Conversion circuit for signed 2's complement to/from signed magnitude. Method uses same circuit to convert 1 011100111001010 to 1 100011000110101. Sign bit determines if inversion is necessary by being tied to select input C of all 0/1 elements. It is also used as carry bit of least significant adder to perform addition. If binary number is positive (sign bit is 0), 0/1 elements (74H87) let number pass through and addition of 0 (sign bit) leaves number unchanged

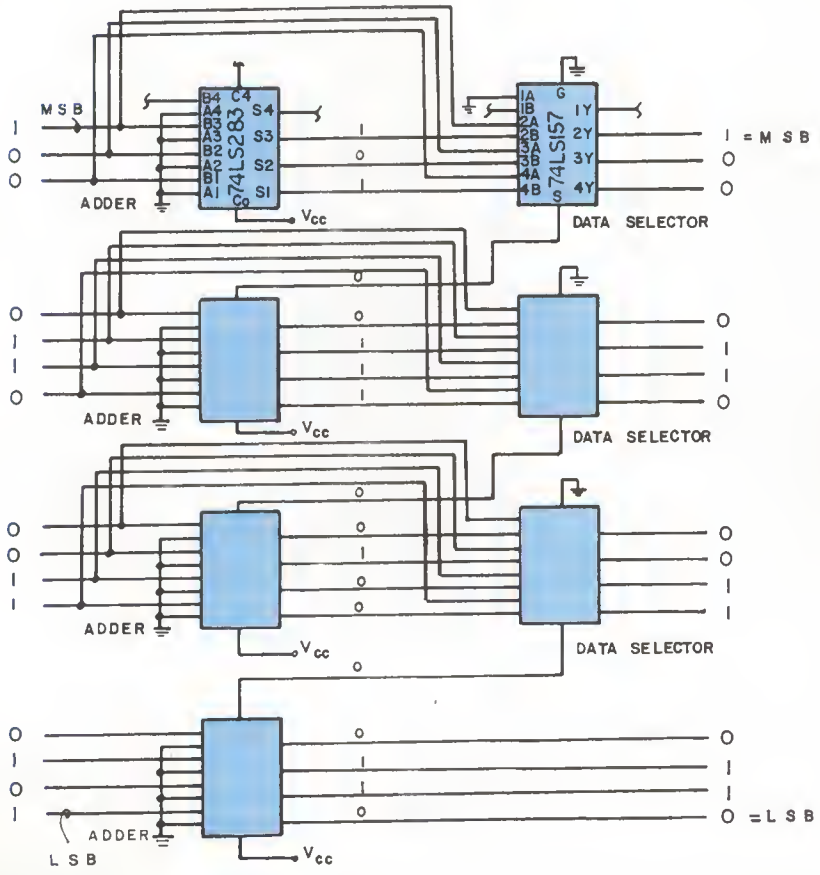

Fig 2 Improved adder circuit. Each adder individually adds 1, and carry of less significant adder selects whether original data or sum of next adder is used. Propagation delay, therefore, is equal to that of one adder and data selector, which is typically 24 ns for a low power Schottky IC, no matter how wide the binary number

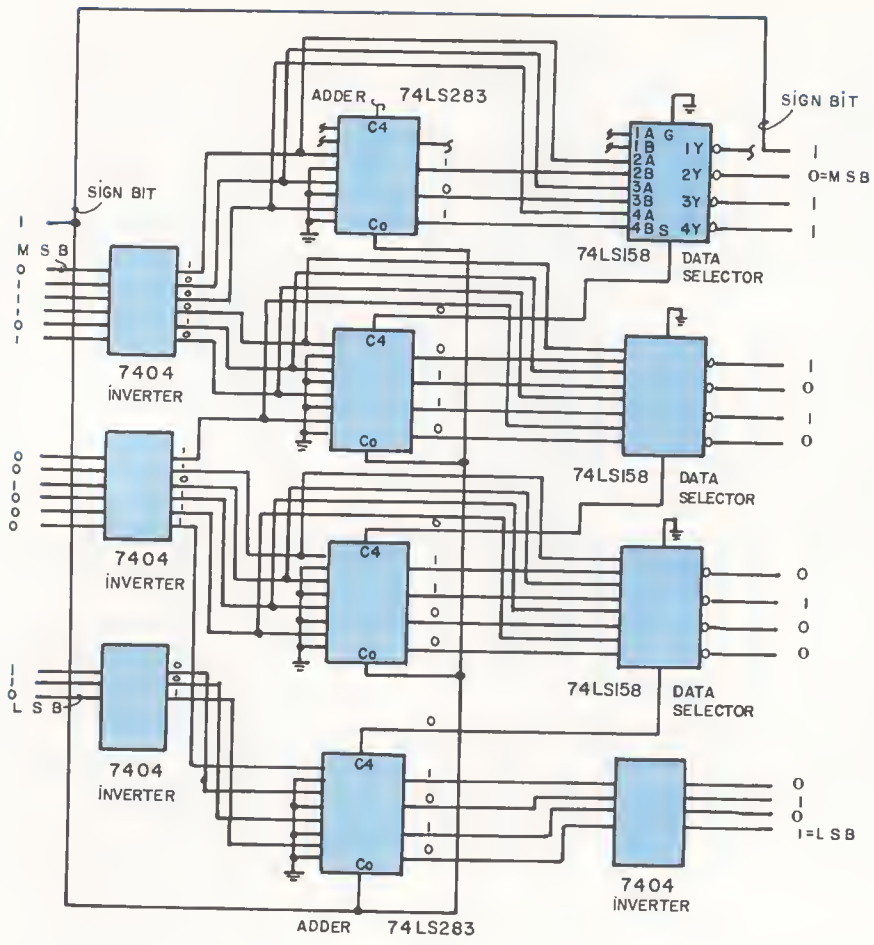

Fig 3 Synchronous conversion of 2's complement to 1's complement. With either positive or negative binary number, conversion requires three steps: invert, add, and invert again. Addition uses high speed circuit of Fig 2, except that data selectors are inverted types (74LS158). For positive numbers, invert, add 0, and invert leaves number unchanged; for negative numbers, invert, add 1, and invert performs necessary conversion. Although synchronous conversion is slower than asynchronous it offers predictable timing

most applications, where speed of operation must be predicted precisely to ensure proper timing, synchronous operation is required, and the conversion circuit is used for both positive and negative binary numbers. Again, the sign bit is used not to switch data but to act as a carry bit in the adder stage. For positive binary numbers, the invert, add 0, and invert conversion process leaves the number unchanged. For negative binary numbers, the invert, add 1, and invert process performs the necessary steps. Note that using inverted type data selectors at the final stage eliminates the need for additional inverter gates (Fig 3).

Overflow in Addition

Addition of two 2's complement binary numbers always ignores the resulting carry, and the sum always has its sign bit at the most significant bit position. However, overflow may result if the sum exceeds the range that can be represented by the number of bits.

Consider a field of eight bits with the most significant bit serving as the sign bit. In this case, the maximum decimal number that the signed 2's complement number can represent is 127 (maximum positive) or −127 (maximum negative). If −82 (decimal) is added to −75 (decimal), the correct sum should be −157 (decimal); however, the sum is out of computational range, yielding an erroneous result.

82_{10} = 0 1010010 Positive 2's complement
-82_{10} = 1 0101110 Negative 2's complement
75_{10} = 0 1001011 Positive 2's complement
-75_{10} = 1 0110101 Negative 2's complement

Addition of −82 and −75 gives

```
    1  0101110  (−82)   If addition rule is applied (ignore result-
+   1  0110101  (−75)   ing carry bit), a wrong answer results
   10  1100011  (+99)   WRONG ANSWER
   ↑↑
Carry Sign
bit   bit
```

However, if 82 is added to −75, the correct sum is 7. This result is in the range of the 8-bit field, and, therefore, the normal addition rule applies.

```
    0  1010010  (+82)   Normal addition rule applies, giving
+   1  0110101  (−75)   correct answer
   10  0000111  (+7)    CORRECT ANSWER
   ↑↑
Carry Sign
bit   bit
```

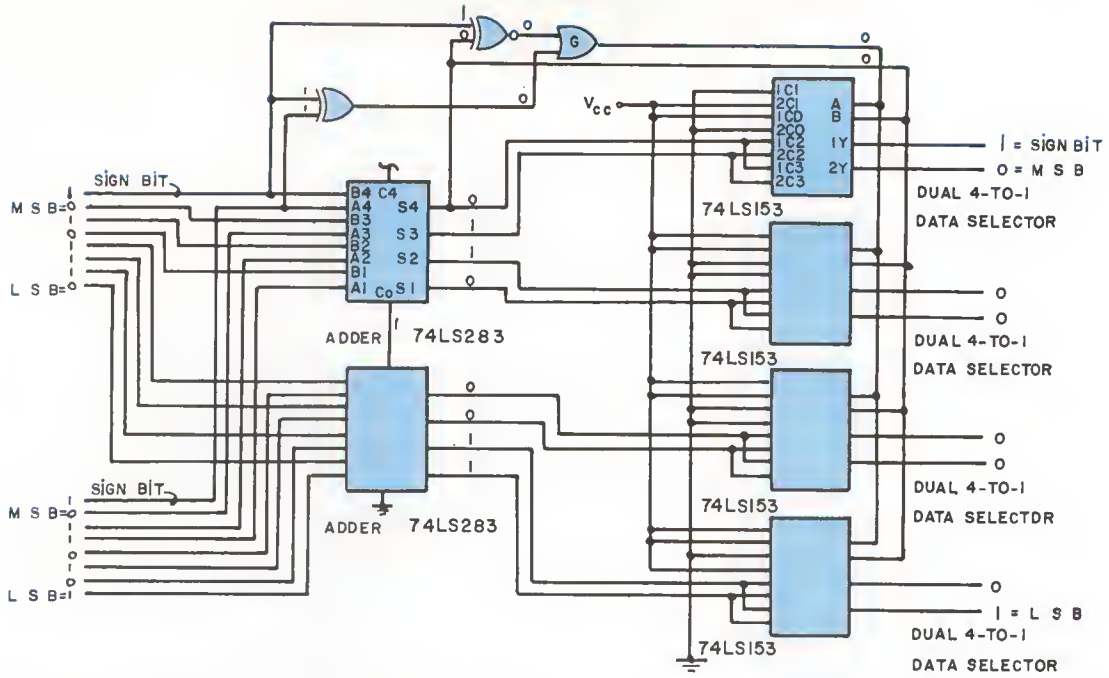

Fig 4 Overflow detector circuit. When addition of two positive numbers produces negative number, or two negative numbers produce positive number, overflow is detected. When detected, output sum is forced through 4-to-1 data selector scheme and is represented as either negative or positive maximum, depending on sign bit. For example, addition of 1 0101110 and 1 0110101 results in overflow; therefore data selectors switch to maximum negative 1 0000001

When overflow does occur, the recommended solution is to force the sum to its maximum value (either positive or negative) to avoid halting the computation process. A detector should be able to perceive this overflow condition and force the sum to its maximum positive or negative value, depending on the sign bit, by examining the sign bits. If two binary numbers are of different signs, their sum is always within range, and no correction is needed. If two binary numbers are of the same sign, overflow occurs either when the sum is positive for two negative numbers, or when the sum is negative for two positive numbers.

In an 8-bit detector circuit (Fig 4) the sign bits of two binary numbers are examined first. Then, in conjunction with the sign bit of the sum, the data selector (74153) switches data either to maximum positive, to maximum negative, or to pass through, according to the following truth table, where X = don't care.

Sign Bits of Two Binary Numbers		Sign of Sum	Result Condition	Data Representation
0	0	1	Overflow	0 1111111 (max pos)
1	1	0	Overflow	1 0000001 (max neg)
0	0	0		
1	1	1	Within Range	Allow result to pass through
0	1	X		
1	0	X		

In this example, the data selector truth table is

A	B	Output
1	X	Pass through
0	0	1 0000001
0	1	0 1111111

Predetermined maximum positive and maximum negative binary numbers are hardwired at the input of the data selectors (74153). Since a 74153 selects one pair of bits out of four pairs of bits, for an 8-bit detector, four selectors are required. Although this appears to be excessive hardware, operational speed is optimized.

The circuit in Fig 4 presents an overflow condition as the result of the addition of 1 0101110 (-82_{10}) and 1 0110101 (-75_{10}). The sign bit of the resulting sum (0, in this example) is fed to select input B of all the 74153s. Output of OR gate G is 0, which is the result of logical manipulation of the two sign bits and the sum sign bit. This output selects input A of all 74153s. Since A and B are both 0, all 74153s switch to the hardwired maximum negative (1 0000001).

Magnitude Comparison For Signed 2's Complement Numbers

Since an IC comparator (eg, 7485) processes only signed magnitude numbers, two signed 2's complement numbers must be converted to magnitude formats before

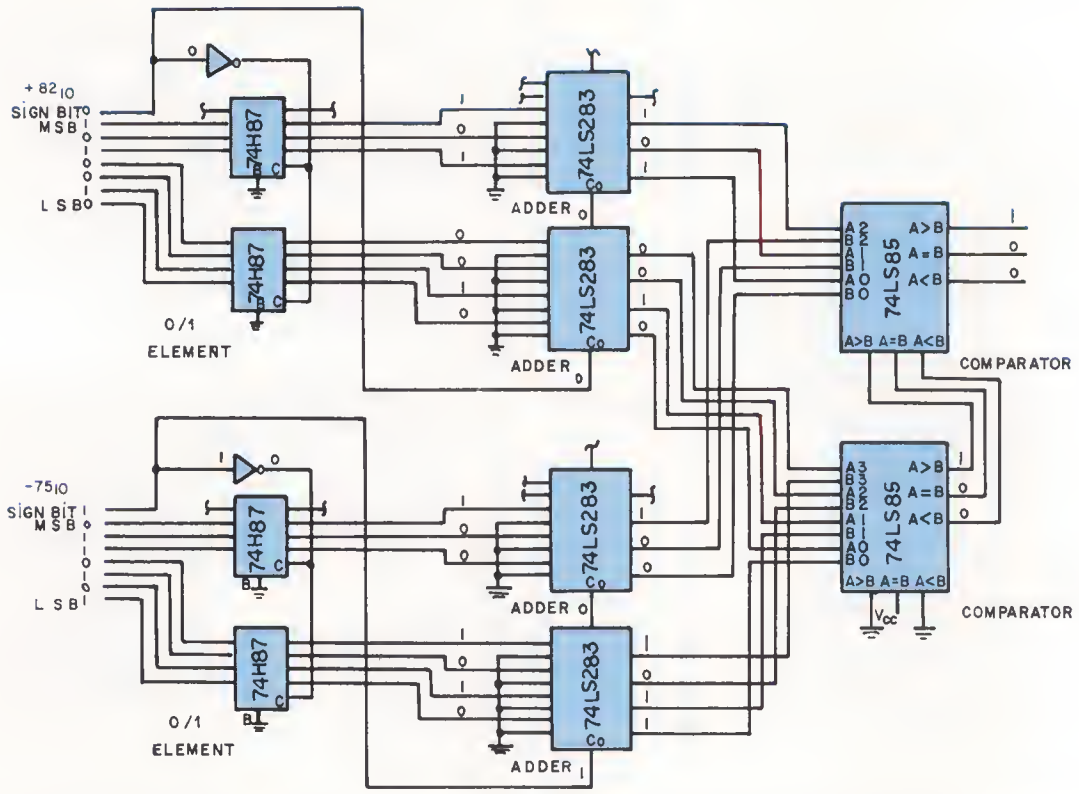

Fig 5 Magnitude comparison using standard IC comparators (7485). Conversion to signed magnitude number is needed before actual comparison. Conversion can use adder circuit configuration of either Fig 1 or 2. For wider word sizes (greater than 16 bits), comparison may require excessive hardware, and propagation delay is increased (unless high speed circuit of Fig 2 is used)

magnitude comparison. Fig 5 illustrates a scheme to perform this number conversion and comparison. The sign bits of two 2's complement numbers are used to determine if inversion is required by feeding to input C of the 0/1 element. The sign bits are also used as carry bits to the adder to perform the necessary conversion to signed magnitude format. Outputs of the adders are in magnitude format (the sign bit is, of course, not used) and are ready for the magnitude comparison. Total propagation delay is equal to the delay in the 0/1 elements (74H87) plus add and compare times. Obviously, if the number of bits is large (16 bits or more), the total delay due to adders and associated hardware might be a problem. As an example, a 16-bit magnitude comparison using this configuration requires approximately 107 ns. The high speed addition scheme presented in Fig 2 can be used, but again the additional hardware is undesirable. To increase speed without increasing hardware, a magnitude comparison scheme for 2's complement numbers has been devised.

Let X and Y be two m-bit 2's complement binary numbers that are to be compared. (In performing the expansion we have ignored convention for clarity.)

$$X = -x_{m-1}2^{m-1} + \sum_{i=0}^{m-2} x_i\, 2^i \qquad (1)$$

$$= -x_{m-1}2^{m-1} + x_{m-2}2^{m-2} + x_{m-3}2^{m-3} + \ldots + x_0 2^0$$

$$Y = -y_{m-1}2^{m-1} + \sum_{i=0}^{m-2} y_i\, 2^i \qquad (2)$$

$$= -y_{m-1}2^{m-1} + y_{m-2}2^{m-2} + y_{m-3}2^{m-3} + \ldots + y_0 2^0$$

To perform a magnitude comparison, take the magnitudes of X and Y, then subtract $|Y|$ from $|X|$ and determine whether the difference is greater than, less than, or equal to 0. In the following discussion, only greater inequality is used since the other two conditions can be similarly derived.

The magnitudes of X and Y in Eqs (1) and (2), respectively, are obtained as follows:

$$|X| = \begin{cases} x_{m-1}2^{m-1} - \sum_{i=0}^{m-2} x_i 2^i & \text{if } x_{m-1} = 1 \\ \sum_{i=0}^{m-2} x_i 2^i & \text{if } x_{m-1} = 0 \end{cases} \quad (3)$$

$$|Y| = \begin{cases} y_{m-1}2^{m-1} - \sum_{i=0}^{m-2} y_i 2^i & \text{if } y_{m-1} = 1 \\ \sum_{i=0}^{m-2} y_i 2^i & \text{if } y_{m-1} = 0 \end{cases} \quad (4)$$

From this the following two cases evolve. For case 1, $x_{m-1} = y_{m-1}$, then

$$|X| - |Y| = \begin{cases} \sum_{i=0}^{m-2} y_i 2^i - \sum_{i=0}^{m-2} x_i 2^i \text{ if } x_{m-1} = y_{m-1} = 1 \\ \sum_{i=0}^{m-2} x_i 2^i - \sum_{i=0}^{m-2} y_i 2^i \text{ if } x_{m-1} = y_{m-1} = 0 \end{cases} \quad (5)$$

which gives

$|X| > |Y|$ if

$$\sum_{i=0}^{m-2} y_i 2^i > \sum_{i=0}^{m-2} x_i 2^i \quad \text{for } x_{m-1} = y_{m-1} = 1 \quad (6)$$

or

$$\sum_{i=0}^{m-2} x_i 2^i > \sum_{i=0}^{m-2} y_i 2^i \quad \text{for } x_{m-1} = y_{m-1} = 0 \quad (7)$$

Therefore, the comparison of $|X|$ and $|Y|$ reduces to the comparison of

$$\sum_{i=0}^{m-2} y_i 2^i \text{ and } \sum_{i=0}^{m-2} x_i 2^i$$

which involves only $(m - 1)$ bits. Comparison is done by using standard ICs (7485) and examining the sign bits to interpret the corresponding results, since inequalities change to the opposite when the sign bits change sign.

For case 2, $x_{m-1} \neq y_{m-1}$, there are two additional situations: (a) $x_{m-1} = 0$, $y_{m-1} = 1$ and (b) $x_{m-1} = 1$, $y_{m-1} = 0$. For case (a)

$$\begin{aligned} |X| - |Y| &= \sum_{i=0}^{m-2} x_i 2^i - y_{m-1}2^{m-1} + \sum_{i=0}^{m-2} y_i 2^i \\ &= -y_{m-1}2^{m-1} + \sum_{i=0}^{m-2} (x_i + y_i)\, 2^i \end{aligned} \quad (8)$$

or $|X| > |Y|$ if

$$\sum_{i=0}^{m-2} x_i 2^i + \sum_{i=0}^{m-2} y_i 2^i > y_{m-1}2^{m-1} \quad (9)$$

To determine whether or not $|X|$ is greater than $|Y|$, first add

$$\sum_{i=0}^{m-2} x_i 2^i \text{ to } \sum_{i=0}^{m-2} y_i 2^i$$

then compare the resulting sum with $y_{m-1}2^{m-1}$. The magnitude comparison is theoretically done by one addition and one comparison in signed magnitude format. However, standard magnitude comparison is not needed, because as shown in Eq (9), y_{m-1} is the mth bit and, therefore, its position in the number format is equivalent to that of the carry bit resultant of the addition. To demonstrate this principle, compare the sum of two 3-digit decimal numbers with a 4-digit decimal number (eg, 1000). If the sum of two 3-digit decimal numbers does not produce a carry, it is obviously less than the 4-digit decimal number. If the sum does produce a carry and if its three less significant digits are greater than 000, that sum is greater than 1000. Equivalently, binary comparison is not required in Eq (9) since the carry bit from the adder and the remaining sum can be checked to see if they exceed $y_{m-1}2^{m-1}$ by the following rule: If the addition produces no carry, the total sum is less than $y_{m-1}2^{m-1}$; if the addition does produce a carry and any of the resulting $(m - 1)$ bits, excluding the carry bit, is a 1, the sum is greater than $y_{m-1}2^{m-1}$; and if none of the $(m - 1)$ bits is a 1, the sum is equal to $y_{m-1}2^{m-1}$.

Therefore, only one addition is required, and the comparison is carried out easily by logical manipulations on the carry bit, the ORed-sum bit (OSB), and the two sign bits (x_{m-1} and y_{m-1}).

For case (b), where $x_{m-1} = 1$, $y_{m-1} = 0$

$$|X| - |Y| = x_{m-1}2^{m-1} - \left[\sum_{i=0}^{m-2} x_i 2^i + \sum_{i=0}^{m-2} y_i 2^i\right] \quad (10)$$

or

$$|X| > |Y| \text{ if } \sum_{i=0}^{m-2} x_i 2^i + \sum_{i=0}^{m-2} y_i 2^i < x_{m-1}2^{m-1} \quad (11)$$

As in case (a), only one addition is required.

For magnitude comparison of signed 2's complement binary numbers using standard magnitude comparators (7485) and adders (74283), the Truth Table exists where X = don't care.

Fig 6 shows a possible implementation of the preceding truth table. The ORed-sum operation can be done in blocks of four bits, corresponding to one adder, and cascading the OR gates. The inverters and the AND-OR gates could be integrated into a custom IC, which would further reduce chip count. Comparison and addition are performed simultaneously and, therefore, the total propagation delay is equal to either the add time or the compare time, whichever is longer (depending on number of bits, compare time may be longer or shorter than add time), plus the ORed sum and the INVERTER-AND-OR gates. Note that no matter how many bits are involved, the number of INVERTER-AND-OR gates is always the same. Therefore, for a large number of bits (24 or more), the savings in hardware and speed are significant. A 24-bit magnitude comparison of signed 2's complement numbers would need only 6 comparators (7485), 6 adders (74283), 6 quadruple OR gates, and a custom IC (or regular small scale integrated circuit). Total comparison time would be approximately 105 ns.

Summary

Possible solutions to three common problems that have been identified in the hardware design and implementation of 2's complement arithmetic are particularly relevant in high speed applications such as fast Fourier transform, digital speech processing, digital pattern recognition, and data acquisition. Because format conversion requires an addition which may have a long delay if the number of bits is greater than 16, a high speed addition circuit is used to reduce the

Truth Table

Sign Bits		Adder		Comparator			Result		
x_{m-1}	y_{m-1}	Carry	OSB	X < Y	X = Y	X > Y	|X| < |Y|	|X| = |Y|	|X| > |Y|
0	0	X	X	1	0	0	1	0	0
0	0	X	X	0	1	0	0	1	0
0	0	X	X	0	0	1	0	0	1
1	1	X	X	1	0	0	0	0	1
1	1	X	X	0	1	0	0	1	0
1	1	X	X	0	0	1	1	0	0
0	1	0	X	X	X	X	0	0	1
0	1	1	0	X	X	X	0	1	0
0	1	1	1	X	X	X	1	0	0
1	0	0	X	X	X	X	1	0	0
1	0	1	0	X	X	X	0	1	0
1	0	1	1	X	X	X	0	0	1

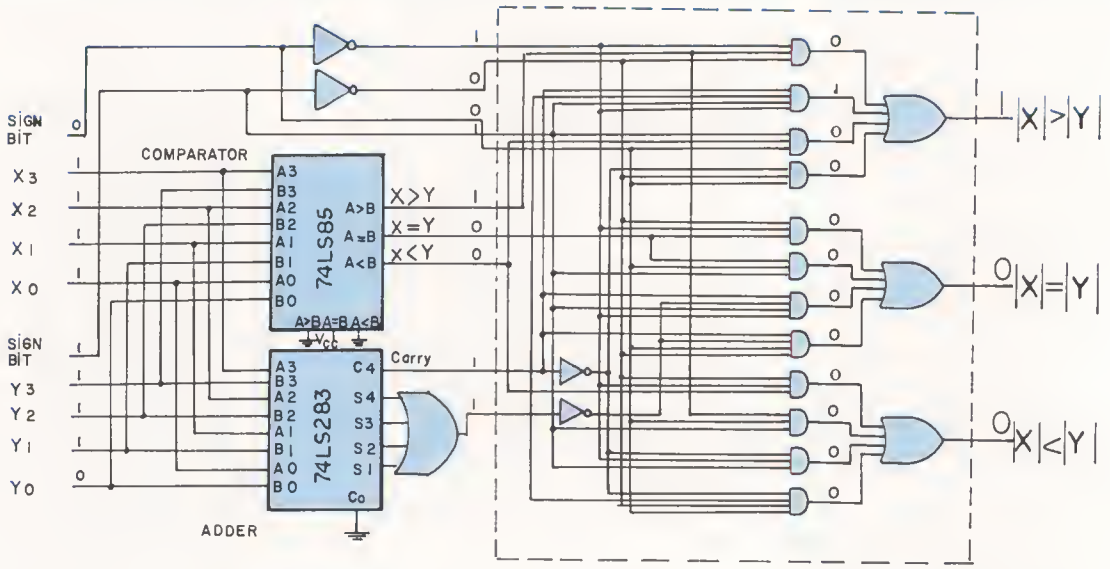

Fig 6 Improved magnitude comparison circuit. Magnitude comparison is performed by either comparison or addition. Propagation delay is therefore equal to delay in comparators or adders, whichever is larger. Logical manipulations are performed in last stage to give correct result. Logical gates could be integrated into custom IC for use in conjunction with existing comparators and adders to increase speed and reduce hardware

add time to 24 ns regardless of how many bits are processed. Overflow condition from addition is detected by observing two sign bits and the resulting sign bit; a circuit detects this condition and forces the sum to its maximum value (negative or positive). Magnitude comparison presents difficulties since commercial ICs are available only for signed magnitude systems (eg, 7485). However, a comparison scheme for 2's complement numbers is demonstrated that can perform the comparison with higher speed and less hardware.

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Thinh V. Nguyen received the BSEE degree from the University of California, Irvine and is completing requirements for the MSEE at the University of Southern California. His research interests include digital signal processing, pattern recognition, robotics, and microcomputer applications. As a project engineer at ITT General Controls, Thinh V. Nguyen is presently responsible for design and development of microcomputer controlled residential products.

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CIRCLE 48 ON INQUIRY CARD

DESIGN NOTE

Cost-Effective 64-Channel Multiplexer System

System design solves full duplex high speed communication problems between multiple terminals and timeshared interactive computers. Link interfacing between host and multiplexer is accomplished via two wires through one host port with minimal I/O overhead

Nishan Urkumyan Shugart Associates, Sunnyvale, California

A microprocessor based multiplexer system has been designed to concentrate up to 64 EIA RS-232-C compatible terminals onto a single 2-way high speed transmission line for a timesharing host computer (Fig 1). Each terminal has 128-char first-in first-out buffered output and character-by-character input, relieving the host of much of the multiplexing task. Fast, serial programmable data communications between host and multiplexer are at rates selectable from 300 to 9600 baud in full-duplex mode using a 68B00 microprocessor (2-MHz version), 68B50 asynchronous communication interface adapter, and fast random access memory

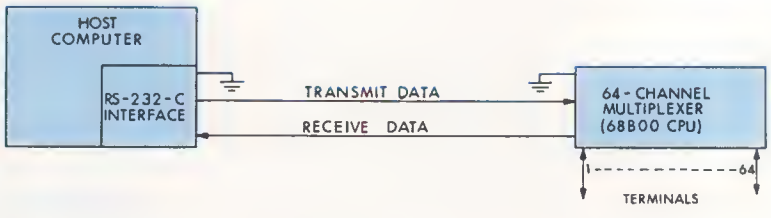

Fig 1 Host to multiplexer link. System shows link via two transmission lines. Up to 64 terminal lines may operate in any mix of baud rates from 300 to 9600 in groups of 8 per I/O module

(2114-2). Cost of providing this multiplexing function is $40 per data channel per input/output card, compared to approximately $300 for existing commercial designs. In high volume production, cost per data channel could easily decrease to $25 per channel.

Design Considerations

Connecting up to 64 terminals to a host computer requires complex hardware and software design considerations involving central processor unit (CPU) run time, system interfacing, interrupt handling, and programming overhead per input/output (I/O) channel. However, a microprocessor based multiplexer (MUX) system overcomes these problems and reduces both cost and I/O management time by assuming the I/O overhead and extra hardware load of the host.

System requirements dictate that all 64 terminals must be processed at the fastest output rate possible. By using fast CPU, random access memory (RAM), and read only memory (ROM) with the MUX, data transfer and receive are performed within 100 μs per terminal (worst case), including host interrupt servicing. All system terminals are polled once every 7 ms (worst case); that is, all terminals are receiving and transmitting simultaneously. Thus, for 64 terminals, a maximum of seven interrupts occur during each poll time. Adding the interrupt handler time (50 μs) to the polling time yields 6.7 ms for one pass, or 149 char/s I/O time per data terminal serviced by the MUX. Terminal processing is held at 9600 baud (approximately 1 char/ms) for fast teletypewriter (TTY) buffer emptying.

Host I/O to the MUX is interrupt serviced. If the host is transmitting data at 9600 baud to the MUX, during every ms the MUX is interrupted to service incoming data. If the terminal buffer is full, a buffer-full character*, followed by the tag for that specific terminal, is transmitted to the host.

Hardware Architecture

Each TTY based terminal connects to a single asynchronous communication

*ASCII character "?," with most significant bit set to "1," is the buffer-full character sent from MUX to host.

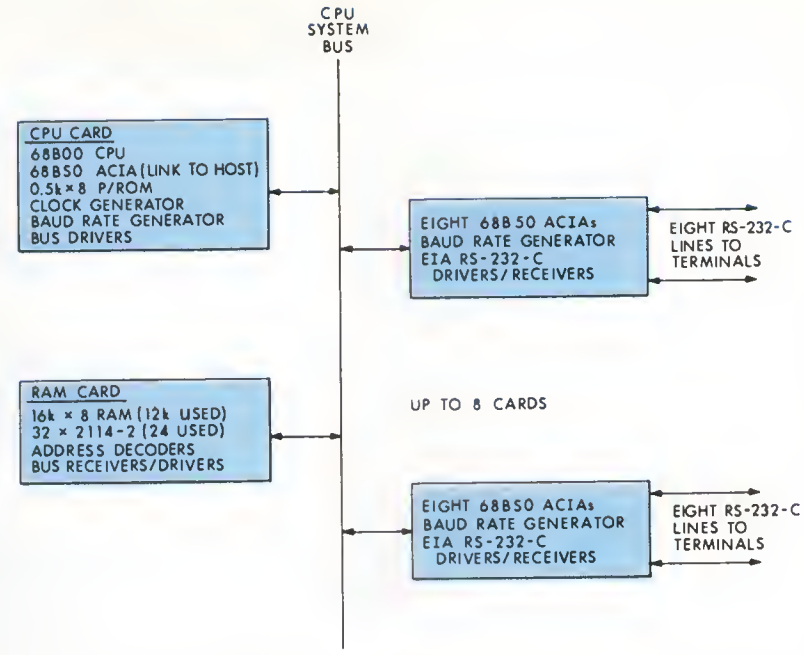

Fig 2 Internal architecture. Interface to host and system program memory are mounted on CPU board. For maximum load, 12k RAM is required; for 32 terminals 8k RAM is sufficient. System software determines how many terminal boards and ACIAs are physically connected; thus, boards or ACIA chips can be removed for maintenance without disabling entire system

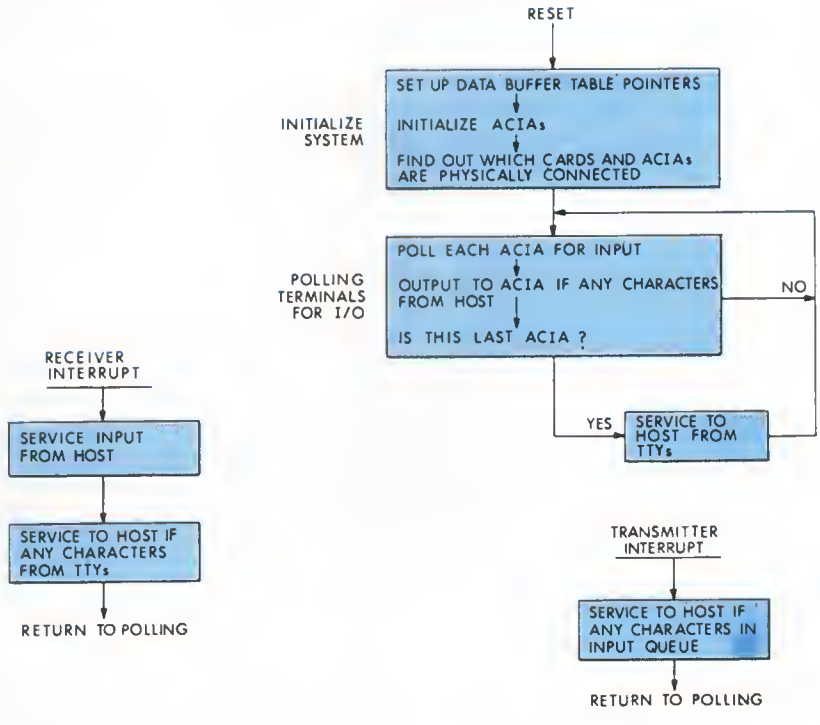

Fig 3 System software. In addition to initilization routine, software performs two simple routines: polling ACIAs for I/O and receiving interrupt to service data from host

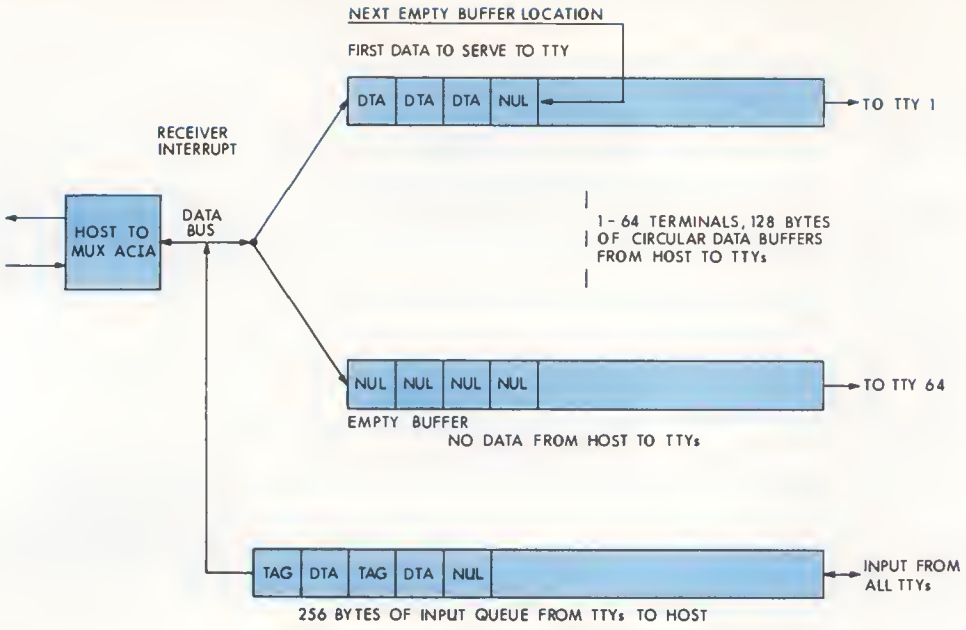

Fig 4 Address processing. Addressing information is transmitted to host with data each time for demultiplexing purposes. Demultiplexing rule can be dynamically updated for additional or fewer terminals upon reset. Receiver Interrupt obtains data from host and places data in appropriate TTY output buffer. Same interrupt routine also services TTY input buffer to host. Therefore, fast I/O rate is produced between host and multiplexer

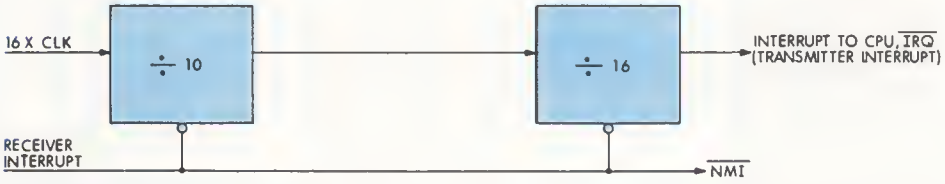

Fig 5 Transmitter interrupt. This interrupt is generated every ten times bit rate to empty input queue. Since receiver interrupt services both receive and transmit, transmitter interrupt is reset to stop false interrupts

interface adapter (ACIA) (Fig 2). Groups of eight ACIAs per card and eight I/O cards service all 64 terminals. These cards are tied to the 68B00 bus. The CPU card has an ACIA for host communication, a 68B00 CPU, and a 512 x 8 programmable ROM (P/ROM). The RAM card consists of 12k x 8 fast static RAMs (24 x 2114-2). Up to 8192 bytes of this RAM are allocated to terminal data output buffering, with a 128-char buffer associated with each terminal. A 256-byte buffer area is reserved for the output queue to the host.

The complete software program for the MUX divides into three parts: initialize, poll, and receiver/transmitter interrupts (Fig 3). Initialization runs only upon reset, which resets all buffer pointers, clears terminal buffers, and determines which cards or ACIAs are physically installed. The active ACIA table is set during initialization by storing only the addresses of the ACIAs that are actually plugged into the system, yielding faster polling during data transmission. Also, the initialization routine sets the stack pointer, resets and sets the ACIAs for speed and number of bits per word, and resets the global pointers.

During polling, each terminal TTY obtains CPU service access for input and output through the active ACIA list set up by initialization. When data are available from the TTY, the tag and data received are stored in the input queue. Then the TTY output buffer is serviced and all pointers are updated. Data to host and data to TTY are all serviced within 100 μs (Fig 3). When there are no incoming characters, and no output buffer is full, the MUX still polls each ACIA.

The receiver interrupt routine obtains data from the host ACIA (Fig 4). If the most significant bit (MSB) is 1, information is handled as a tag; if MSB is 0, information is stored in the TTY buffer pointed to by the tag

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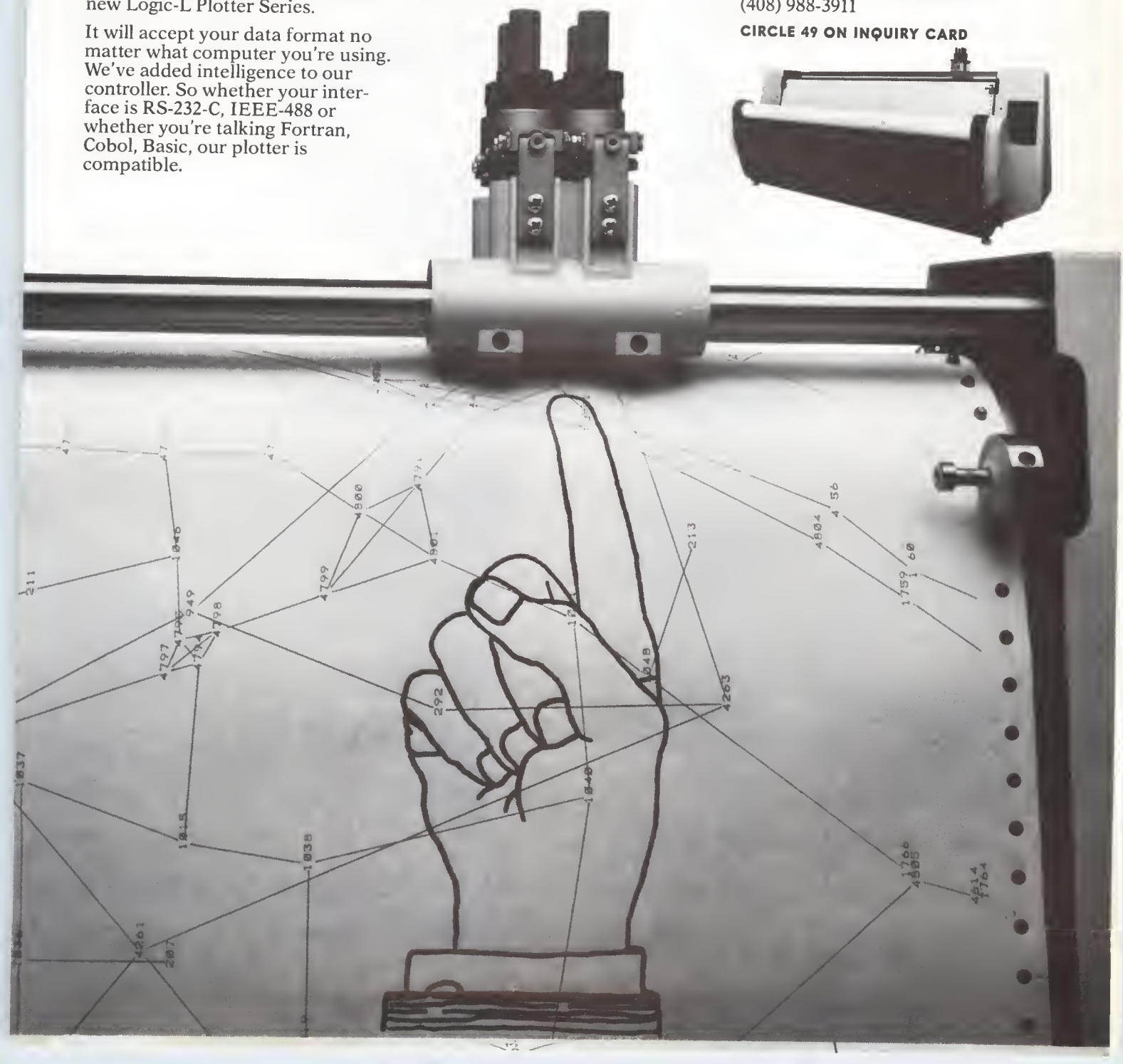

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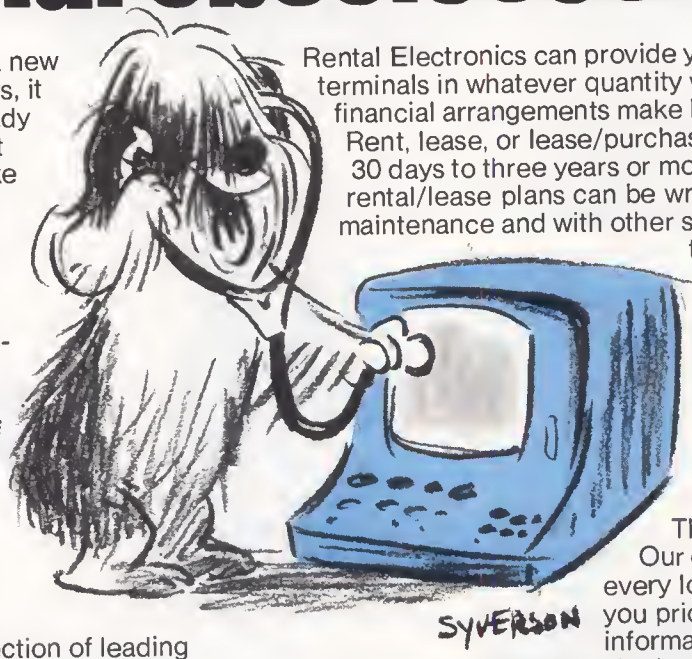

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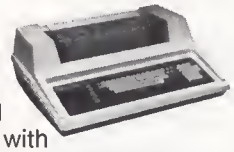
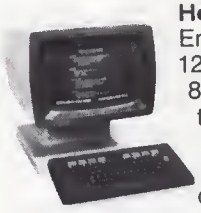


TI Model 820 Keyboard Send-Receive Data Terminal/Printer Printer operates at 150 cps on 9 x 7 wire matrix assembly printhead. Full ASCII Keyboard (ANSI-compatible) with N-key roll over. Operates in Asynchronous, USASCII, RS232C interfaces and is compatible with Bell 103, 113, 202 and 212 units. Selectable baud rates of 110 to 9600.



Hewlett-Packard 2621A/P Terminals Enhanced 9 x 15 dot character cell, full 128-character ASCII character set in 24 80-character lines. Two pages of continuously scrolling memory. RS232C and Bell 103A compatible. 110 to 9600 baud. 2621/P includes built-in printer operating at 120 cps.

Tally T-2000 Hush-Tone Line Printer Acoustically designed enclosure. Operates at 125 (Model 2100) and 200 lines/minute (Model 2200) with standard 64 character USASCII. Line spacing switch selectable, 6 or 8 per inch.

ADDS Regent 200 Terminal 24 lines x 80 characters, 25th "status" line shows operating mode. 128 character ASCII. RS232C/CCIT V.24 communications interface operating 75 to 19.2 BPS, switch selectable. Buffered transmission, auxiliary ports.

Beehive Micro B 1A Terminal 128 ASCII character set; switch selectable scroll/non-scroll mode; X-Y addressing; 24 x 80 display format; single key memory lock; fully buffered communications to auxiliary peripheral device.

Lear Siegler ADM-3A Data Entry Display Terminal 12" diagonal, 24-line screen. 64 ASCII characters. Full or half duplex operating modes, switch selectable, baud rates from 75 to 19,200. RS232C interface, 20mA current loop.

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Handshaking Between Host and MUX

Host Initiated Commands	
1 1 • • • • • • •	This is a tag byte; MSB = 1, bits 0 - 7 are tag, following byte is data
1 0 1 1 1 1 0 1	Host requests number of terminals on MUX and their tags
0 • • • • • • •	Data byte from host; MSB = 0
0 0 0 0 0 0 0 0	Null characters, no printing, no data characters
MUX to Host Commands	
1 0 1 1 1 1 1 1	Buffer-full characters for terminal indicated in following tag byte
1 0 1 1 1 1 0 0	Next tag is first TTY in system followed by remaining tags
1 0 1 1 1 1 1 0	End of TTY tags in system
1 1 • • • • • •	Tag byte, following byte is data
0 • • • • • • •	Data byte

Data protocol is used on 8-bit RS-232-C 16 times clock baud rate. This rate is switch selectable from 300 to 9600 baud on each card. Eight bits are used for both tag and data bytes with one stop bit. MSB is utilized for data/tag distinction; other seven bits are ASCII characters

just received. Then, the input queue to the host is serviced. Next, the host channel is busy for the 1-ms time interval needed for one character. Therefore, receive and transmit data from the host are serviced by the same receiver interrupt. Finally, polling resumes as described. Other characters from the host computer determine status requests, number of TTYs, TTY identification tags in the system, and null characters for fast data request (see "Handshaking Between Host and MUX"). After each receiver interrupt, the interrupt vector is updated to handle the next character in order to speed up data transfer. Thus, after servicing a tag from the host, the receiver interrupt vector is updated to handle the next incoming character as data. The receiver interrupt routine can also detect errors during transmission; for example, two data bytes in a row force the MUX to reset itself for a new tag byte.

To speed up and maintain the host/MUX data transmission rate, an internal hardware timer generates a transmitter interrupt every ten times the bit rate, which is the transmission rate for eight data bits, one start bit, and one stop bit, during asynchronous communication per data byte (Fig 5). This interrupt is reset by the receiver interrupt if data are received from the host; otherwise, the counter generates an interrupt in the MUX to send data from input queue to host.

Summary

Compared with available systems, the described MUX design—power supply, chassis, CPU, 12k x 8 RAM, and eight I/O cards—totals less than $5000, for an average of $70 per terminal with a maximum load of 64 terminals. Major advantage of this system is the tag/data protocol per character. This protocol furnishes fast character response times for the TTYs in full duplex mode. System architecture eliminates the need for a special host interface, which is required in some MUXs to prevent character loss. A tradeoff disadvantage of this MUX is the need for data buffers to hold incoming messages due to polling delays under heavily loaded conditions.

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DESIGN NOTE

Intelligent Controller Increases Data Throughput, Reduces Host Overhead

Dual microprocessors joined by buffer improve throughput, response, and functionality of intelligent controller that interfaces laboratory peripherals and host minicomputer

Charles A. Samuelson Digital Equipment Corporation, Tewksbury, Massachusetts

Laboratory input/output peripherals, such as analog-to-digital and digital-to-analog converters, digital input and output registers, and programmable realtime clocks, are traditionally connected to minicomputers using straightforward program interrupt interfaces. These interfaces issue interrupts for each data point and use system software for control of data transfers. Advantages to this approach include low hardware cost because all intelligence is in system software, program compatibility since major investments in application software are transferrable, and widespread flexibility through specialized software. Conversely, disadvantages are limted hardware and software system performance, devotion of a large share of the controlling minicomputers' resources to data acquisition, and prohibitive costs associated with developing specialized and optimized software for individual laboratory experiments.

The highest priority in designing an intelligent controller system for interfacing realtime laboratory peripherals to a host minicomputer was to cost effectively increase realtime performance while leaving the maximum amount of system resources available for data computation. Realtime system performance has three primary characteristics: throughput, response, and functionality. Throughput is specified as the amount of data that can be moved through a system per unit time, response is defined as the time needed to identify and react to a particular event, and functionality is a measure of the system complexity for the decision making process. The importance of each of these interrelated characteristics varies with the application.

PROMs

ECL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
32 x 8	MCM10139▲	25	ECL output	16
256 x 4	MCM10149▲	30	ECL output	16

TTL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
64 x 8	MCM5503/5303▲	125	Open collector	24
64 x 8	MCM5504/5304▲	125	2K pull-up	24
512 x 4	MCM7620▲	70	Open collector	16
512 x 4	MCM7621▲	70	3-state	16
512 x 8	MCM7640▲	70	Open collector	24
512 x 8	MCM7641▲	70	3-state	24
1024 x 4	MCM7642▲	70	Open collector	18
1024 x 4	MCM7643▲	70	3-state	18
1024 x 8	MCM7680▲	70	Open collector	24
1024 x 8	MCM7681▲	70	3-state	24
2048 x 4	MCM7684*▲	70	Open collector	18
2048 x 4	MCM7685*▲	70	3-state	18
2048 x 4	MCM7686*▲	70	Open collector with latches	20
2048 x 4	MCM7687*▲	70	3-state with latches	20
2048 x 4	MCM7688*▲	----	Open collector with registers	20
2048 x 4	MCM7689*▲	----	3-state with registers	20

EPROMs

MOS EPROMs

Organization	Part Number	Access Time (ns max)	No. of Power Supplies[1]	No. of Pins
1024 x 8	MCM2708C▲	450	3	24
1024 x 8	MCM27A08C▲	300	3	24
1024 x 8	MCM68708C▲	450	3	24
1024 x 8	MCM68A708C	300	3	24
2048 x 8	TMS2716C▲	450	3	24
2048 x 8	TMS27A16C▲	300	3	24
2048 x 8	MCM2716C*▲	450	1	24
2048 x 8	MCM27A16C*▲	350	1	24
8192 x 8	MCM68764C*	450	1	24

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RAMs ROMs PROMs EPROMs

June 1979

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RAMs

MOS DYNAMIC RAMs

Organization	Part Number	Access Time (ns max)	No. of Power Supplies[1]	No. of Pins
4096 x 1	MCM4096C-6▲	250	3	16
4096 x 1	MCM4096C-16▲	300	3	16
4096 x 1	MCM4096C-11▲	350	3	16
4096 x 1	MCM4027AC-2▲	150	3	16
4096 x 1	MCM4027AC-3▲	200	3	16
4096 x 1	MCM4027AC-4▲	250	3	16
4096 x 1	MCM6604AC	350	3	16
4096 x 1	MCM6604AC-2	250	3	16
4096 x 1	MCM6604AC-4	300	3	16
4096 x 1	MCM6605AL	300	3	22
4096 x 1	MCM6605AL-2	200	3	22
16,384 x 1	MCM4116AC-15▲	150	3	16
16,384 x 1	MCM4116AC-20▲	200	3	16
16,384 x 1	MCM4116AC-25▲	250	3	16
16,384 x 1	MCM4116AC-30▲	300	3	16

TTL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
256 x 4	MCM93412*▲	45	Open collector	22
256 x 4	MCM93422*▲	45	3-state	22
1024 x 1	MCM93415▲	45	Open collector	16
1024 x 1	MCM93425▲	45	3-state	16

*To be introduced.
▲Second source.
Heavy black type denotes industry standard part numbers.
Operating temperature ranges:
MOS 0°C to 70°C
CMOS −40°C to +85°C and −55°C to +125°C
ECL Consult individual data sheets.
TTL Military −55°C to +125°C, Commercial 0°C to 70°C

1 MOS power supplies:
3 +12, ±5 V
1 +5 V
All MOS outputs are 3-state except the 6570 and 6580 Series which are open-collector.

2 Character generators include shifted and unshifted characters, ASCII, alpha-numeric control, math, Japanese, British, German, European and French symbols.

MOS STATIC RAMs

Organization	Part Number	Access Time (ns max)	No. of Power Supplies[1]	No. of Pins
128 x 8	MCM6810	450	1	24
128 x 8	MCM68A10	360	1	24
128 x 8	MCM68810	250	1	24
1024 x 4	MCM2114P-20▲	200	1	18
1024 x 4	MCM2114P-25▲	250	1	18
1024 x 4	MCM2114P-30▲	300	1	18
1024 x 4	MCM2114P-45▲	450	1	18
1024 x 4	MCM21L14P-20▲	200	1	18
1024 x 4	MCM21L14P-25▲	250	1	18
1024 x 4	MCM21L14P-30▲	300	1	18
1024 x 4	MCM21L14P-45▲	450	1	18
4096 x 1	MCM6641P-20▲	200	1	18
4096 x 1	MCM6641P-25▲	250	1	18
4096 x 1	MCM6641P-30▲	300	1	18
4096 x 1	MCM6641P-45▲	450	1	18
4096 x 1	MCM66L41P-20▲	200	1	18
4096 x 1	MCM66L41P-25▲	250	1	18
4096 x 1	MCM66L41P-30▲	300	1	18
4096 x 1	MCM66L41P-45▲	450	1	18
4096 x 1	MCM2147C-55*▲	55	1	18
4096 x 1	MCM2147C-70*▲	70	1	18
4096 x 1	MCM2147C-85*▲	85	1	18

CMOS STATIC RAMs

Organization	Part Number	Access Time (ns max)	No. of Power Supplies	No. of Pins
256 x 4	MCM145101-1▲	450	1	22
256 x 4	MCM145101-3▲	650	1	22
256 x 4	MCM145101-8▲	800	1	22
4096 x 1	MCM146504▲	450	1	18
1024 x 1	MCM146508*▲	460	1	16
1024 x 1	MCM146508-1*▲	300	1	16
1024 x 1	MCM146518*▲	460	1	18
1024 x 1	MCM146518-1*▲	300	1	18

ECL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
8 x 2	MCM10143	15	ECL output	24
256 x 1	MCM10144▲	26	ECL output	16
16 x 4	MCM10145▲	15	ECL output	16
1024 x 1	MCM10146▲	29	ECL output	16
128 x 1	MCM10147▲	15	ECL output	16
256 x 1	MCM10152▲	15	ECL output	16

ROMs

MOS STATIC ROMs

Character Generators[2]

Organization	Part Number	Access Time (ns max)	No. of Power Supplies	No. of Pins
128 x (7 x 5)	MCM6670P	350	1	18
128 x (7 x 5)	MCM6674P	350	1	18
128 x (9 x 7)	MCM66700P▲	350	1	24
128 x (9 x 7)	MCM66710P▲	350	1	24
128 x (9 x 7)	MCM66714P▲	350	1	24
128 x (9 x 7)	MCM66720P▲	350	1	24
128 x (9 x 7)	MCM66730P▲	350	1	24
128 x (9 x 7)	MCM66734P	350	1	24
128 x (9 x 7)	MCM66740P▲	350	1	24
128 x (9 x 7)	MCM66750P▲	350	1	24
128 x (9 x 7)	MCM66760P▲	350	1	24
128 x (9 x 7)	MCM66770P	350	1	24
128 x (9 x 7)	MCM66780P	350	1	24
128 x (9 x 7)	MCM66790P	350	1	24

Binary ROMs

Organization	Part Number	Access Time (ns max)	No. of Power Supplies	No. of Pins
1024 x 8	MCM68A30P8	350	1	24
1024 x 8	MCM68A308P7	350	1	24
2048 x 8	MCM68A316P91	350	1	24
1024 x 8	MCM68830AP▲	250	1	24
1024 x 8	MCM68A30AP▲	350	1	24
1024 x 8	MCM68B308P▲	250	1	24
1024 x 8	MCM68A308P▲	350	1	24
2048 x 8	MCM68A316EP▲	350	1	24
2048 x 8	MCM68A316AP▲	350	1	24
4096 x 8	MCM68A332P▲	350	1	24
4096 x 8	MCM68A332P2*	350	1	24
8192 x 8	MCM68A364P*▲	350	1	24
8192 x 8	MCM68A364P3*	350	1	24
8192 x 8	MCM68B364P3*	250	1	24

CMOS ROM

Organization	Part Number	Access Time (ns max)	No. of Power Supplies	No. of Pins
256 x 4	MCM14524	1200	1	16

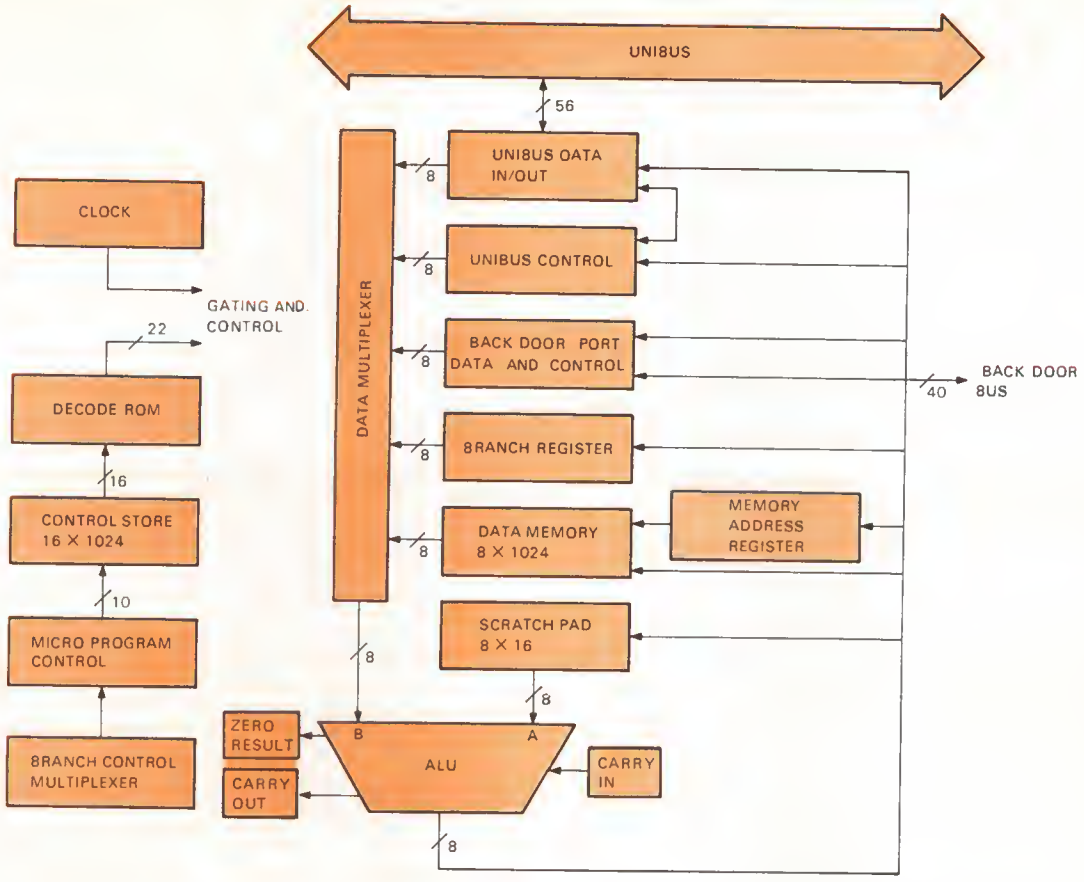

Fig 1 Microprocessor block diagram. Two microprocessors are used in intelligent controller. Included are microprogrammable UNIBUS™ interface and external backdoor interface port. Data are cycled through ALU from either 1 of 16 scratchpad registers or from data multiplexer. Clock gates output from decode ROM, determining interconnection of data paths and ALU functions. Total instruction cycle is 300 ns

For example, throughput rate or response time is generally inversely proportional to functionality.

Design Background

The controller design had to be compatible with program interrupt laboratory input/output (I/O) interfaces already in use with existing laboratory computer systems. This constraint bounded development costs and guaranteed that current laboratory systems could be field upgraded.

Laboratory applications such as digital signal processing and time-series analysis require accurately timed, synchronous transfers of data over long time periods without skipped points. Potentially large (relative to single-point time) latencies exist due to host processor I/O contention and system software overhead. Three design techniques are generally used to overcome this difficulty. Data transfer algorithms may be implemented in a separate, independent processor; blocks of data may be transferred directly to and from host processor memory using direct memory access (DMA); and data blocks in memory may be organized using a multiple buffering scheme. These techniques suggest the concept of a hardware oriented peripheral controller that would provide data transfer algorithms for laboratory I/O peripherals, store and retrieve data from host processor memory, and serve as an intelligent interface to host processor system software.

Due to a concurrent project, a general purpose microprocessor with two interface ports was available. The first port provides a microprogrammable interface to the UNIBUS™ of PDP-11 and VAX-11 host processors. This port provides control and status registers for communication between the host processor software and controller microcode. It permits the microprocessor to generate interrupts to the host software under microprogram control. Through this port the microprocessor can, under microprogram control, use DMA to access the host memory and other peripheral devices on the UNIBUS.

The second interface port creates a simple bus on a 40-conductor ribbon cable. Data and control paths on this "backdoor" bus allow communication with external logic without using bandwidth on the host processor memory bus.

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Containing 8-bit wide data paths, the microprocessor (Fig 1) has 16 scratchpad registers, a 256-word by 8-bit local data memory, and a 1024-word by 16-bit control store. Basic instruction time is 300 ns. The vertically organized microcode is relatively easy to microprogram. There are no multiple-cycle instructions; operands can be addressed and fetched, arithmetic and logical operations performed, and results stored in one operation. In addition, operands can be moved directly from an input port to an output port in one instruction.

Design Implementation

To meet design criteria, two of the microprocessors described previously, a master and a slave, are connected back-to-back with buffer logic. This design comprises the LPA11-K intelligent laboratory peripheral controller (Fig 2). The microprocessors communicate with each other over their second interface ports. Connecting to the host memory and peripheral bus, the master is responsible for starting and stopping requests, transferring data to and from host memory, and reporting status. The slave connects to a second or I/O bus that is identical to the host's memory and peripheral bus, but is electrically separate. The slave controls laboratory peripheral devices by issuing DMA requests to their control and status registers over the I/O bus. It transfers data to (from) the master for storage (retrieval) into host memory.

The interprocessor buffer (IPB) module connects the master and slave and provides data paths for their backdoor ports. The IPB supplies arbitration logic for controlling interrupts and DMA transfers on the I/O bus. Data paths between the two microprocessors contain first in, first out (FIFO) buffer memories, which allow master and slave to communicate with each other without synchronization on each data byte. It also frees them from host I/O latencies. The module monitors the program interrupt request lines on the I/O bus and signals the slave when laboratory peripheral devices need service.

Firmware in both microprocessors defines the controller interface to the host and the data transfer algorithms for the laboratory I/O peripherals. The controller is provided premicroprogrammed, allowing usage with minimal development effort. The master microcode also creates a software interface compatible with the host operating system.

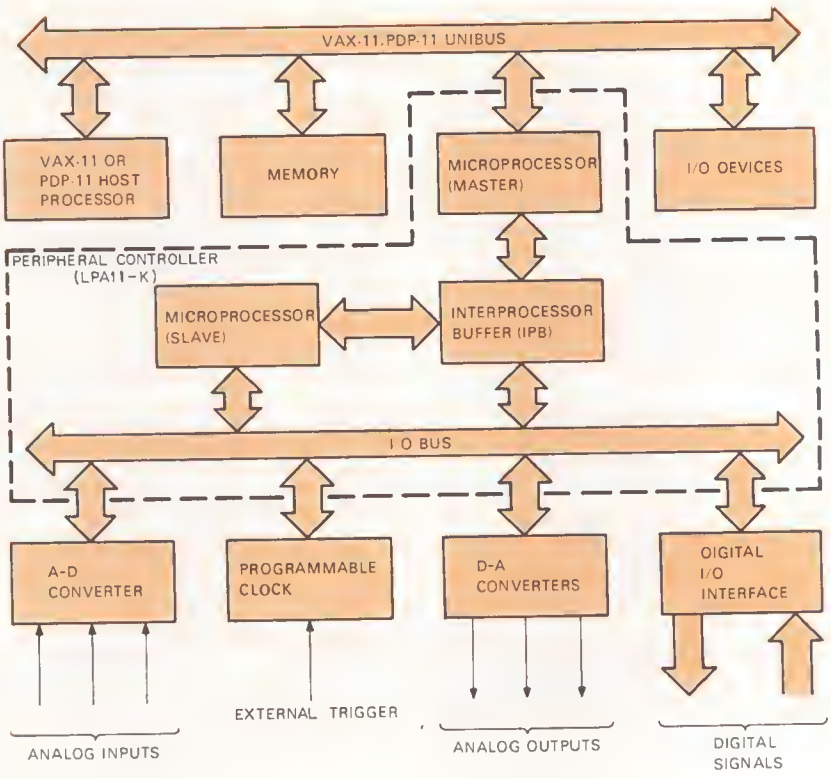

Fig 2 System block diagram. Two microprocessors are interconnected through interprocessor buffer. Master transfers control, status, and data to and from host memory. Slave controls realtime laboratory peripherals' I/O bus. Interprocessor buffer is also I/O bus arbitrator

Two notable properties of the intelligent controller interface are the method by which control information is passed between the host and the controller, and the method by which host memory data buffers are managed. Parameters typically encountered in data acquisition calls include buffer addresses, buffer sizes, laboratory peripheral channel addresses, sample rates, and sample modes. Previously, these parameters were specified in FORTRAN or BASIC calls and processed by assembly language routines. In contrast, the intelligent controller inputs these parameters using DMA and processes them internally. This simplifies programming protocol for host operating system device code; it only needs to specify the address of a parameter list rather than the parameters themselves. A benefit of this design strategy is that the operating system device driver is independent of enhancements to the controller's functionality.

The controller transfers data continuously, storing and retrieving it from multiple buffers in host memory. Only one system I/O request is needed to initiate the transfer of any amount of data. All memory addresses of data buffer areas are specified in the initial I/O request. Thereafter, the controller and the

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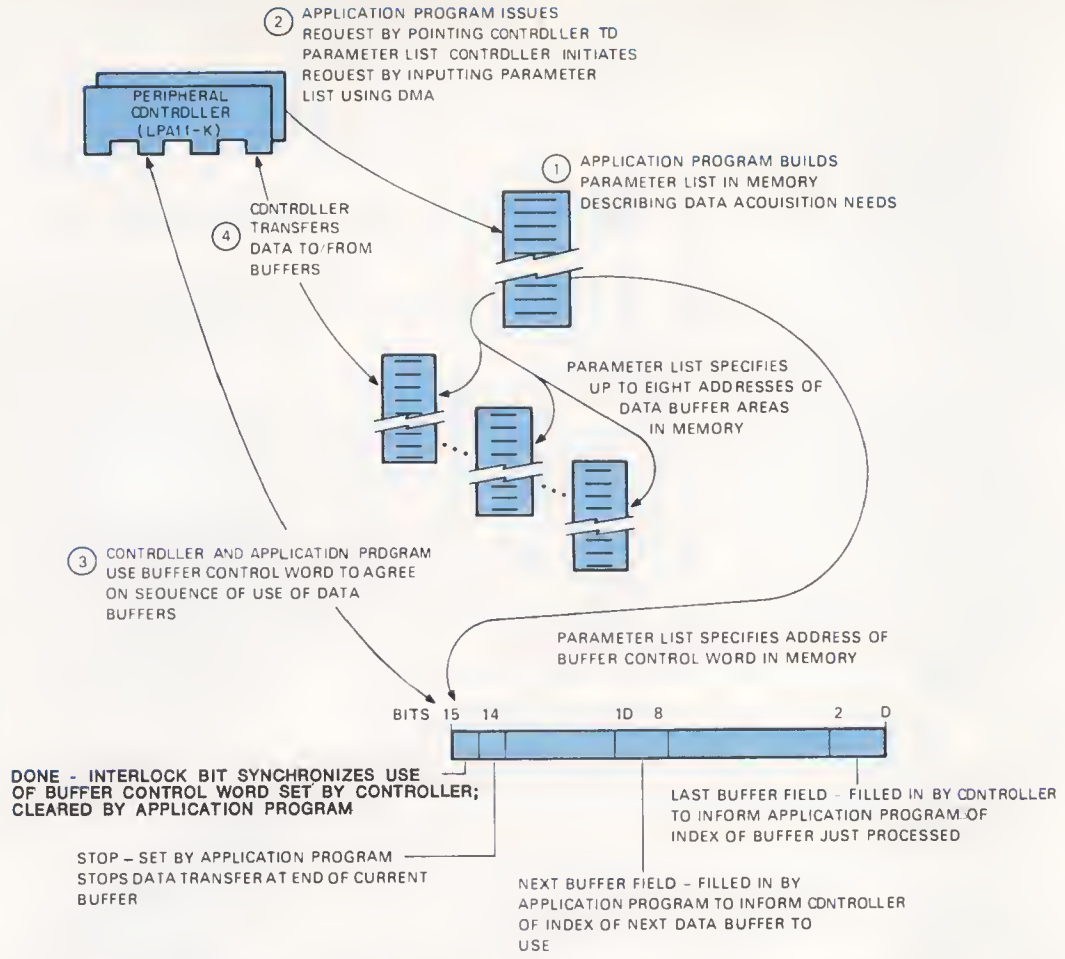

Fig 3 Hardware/software control flow. Flow for starting data transfers and controlling data buffer areas is depicted. Control tables are built by application program and interpreted by intelligent controller. After data transfers commence, controller and application program agree on allocation of data areas through buffer control word

application program specify buffers by an index (0 for the first buffer, 1 for the second, etc). Address validation and relocation are performed only once by the host operating system. Host memory data buffer areas can be reused when data contained in them have been processed. Chaining from buffer to buffer is accomplished using a control word in the application program's memory, specifying the sequence of data buffer usage. The intelligent controller accesses this control word using DMAs when it requires a new data buffer index. Chaining permits the application program to communicate directly with the controller during data acquisition without operating system executive requests (Fig 3).

System Applications

In a typical laboratory application, several experiments are performed simultaneously. Each experimenter wants to transfer data to or from an instrument independently, specifying separate data buffers, sample rates, and I/O peripheral channels. The controller's two operating modes either allow up to eight independent experiments to transfer data or permit high data throughput for a single experiment. Choice of operating modes is one method of addressing the possible tradeoff between throughput and functionality.

Controller design favors throughput-intensive applications. It pipelines data through two microprocessors and FIFO memories into large block buffers in host processor memory. Microcode in the slave provides event detection and synchronization of data transfers with external events. Thus, the burden of starting and stopping the data pipeline is provided by the controller and not by host processor software. Throughput measurements show maximum analog data transfer rates in excess of 150k samples/s in the single experiment mode. This rate can be maintained continuously by a FORTRAN program running on an operating system. Host processor load measurements indicate that about 20% of processor I/O bandwidth is used, leaving 80% of the host available for data processing and computation. □

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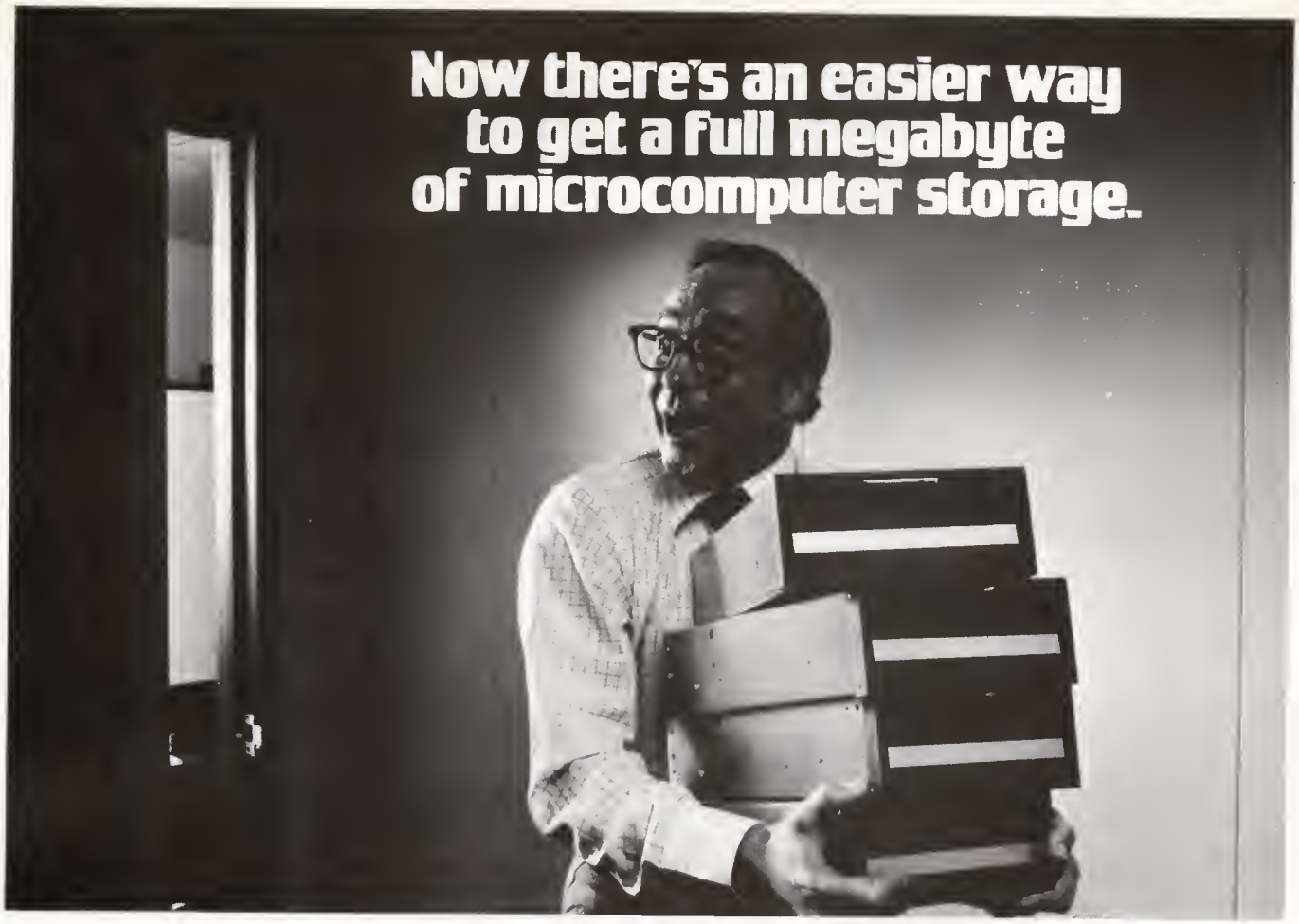

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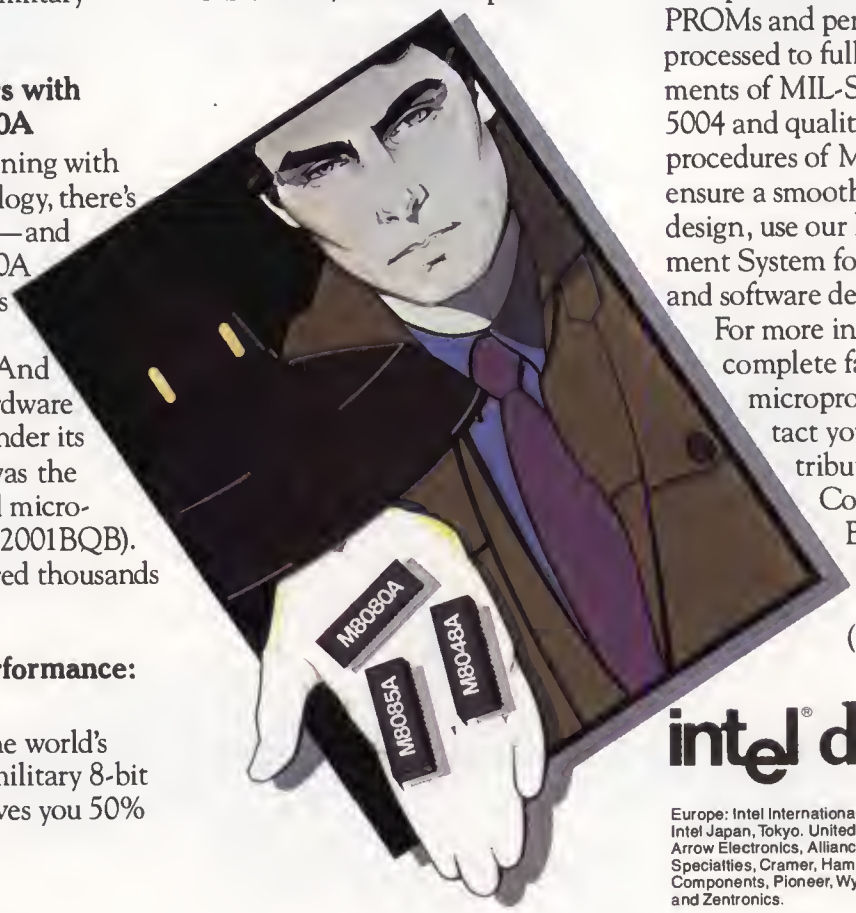

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DESIGN NOTE

Implementation of Division Algorithm Halves Iteration Time

To speed division, nonrestoring divide algorithm executed on a microprocessor based system reduces division iteration time by performing all bit manipulations during one microinstruction

Norton Markin Ministry of Defense, Israel

The division process for binary numbers can be considered to be composed of three steps. In the first step, the validity of the divisor and dividend are checked, ie, whether the divisor is zero or the dividend value is within required limits. During the second step, the iteration is carried out and the quotient and remainder are generated. For the third step, the remainder is processed, any necessary corrections are made to the quotient, and the final quotient is checked to determine whether an arithmetic overflow has taken place. The iteration used in this division process is usually based upon the nonrestoring divide algorithm.[1] In this algorithm, multiples of the divisor are either subtracted or added to the dividend to determine the value of the quotient.

A microprogram to implement the iterative portion consists of at least two microinstructions. The first generates the multiple of the divisor, and determines whether the next is to perform an addition or a subtraction operation. The second microinstruction performs the arithmetic operation to determine the value of a particular digit in the quotient. In the following implementation each iteration is done in only one microinstruction, thereby decreasing iteration time by 50%.

Divide Algorithm

Rules for obtaining the value of a particular bit (Q_N), and generating a new remainder (R_N) using the nonrestoring divide algorithm are as follows:

(1) Generate proper binary multiple D_N, where $D_N = D \times 2^N$.

(2) If sign of R_{N+1} is identical to sign of D_N, subtract D_N from R_{N+1} to form R_N; if not, add D_N to R_{N+1} to form R_N.

(3) If sign of R_N is identical to sign of D_N, Q_N is 1; if not, Q_N is 0.

For these rules, D_N is the value of the binary multiple of the divisor at a particular iteration stage, and R_N is the resulting modified dividend at that iteration stage. Also, the dividend, divisor, quotient, and remainder can be represented as whole numbers (as opposed to binary fractions), and negative numbers are given in their 2's complement form. When dividing a 32-bit binary number by a 16-bit binary number using these rules, N ranges from 15 to 0, where N starts with a value of 15 for the first iteration.

R_{N+1} takes the value of the dividend for the first iteration. Therefore, during that iteration the decision of whether to initially subtract or add D15 to the dividend is a function of both the D15 and the dividend sign bits. If both sign bits are the same, D15 is subtracted from the dividend to form the new modified dividend (R15); otherwise, D15 is added to the dividend to form R15. The result of this add/subtract operation determines the value of the most significant quotient bit (Q15). If the D15 and R15 sign bits are the same, Q15 is a 1; if not, Q15 is a 0.

The second most significant Q bit, and succeeding bits, are determined in a similar manner. Thus, for Q14, the next highest binary multiple ($D14 = D \times 2^{14}$) is either added to or subtracted from the previously modified dividend (R15) to form the new R14 remainder—where a comparison of the sign bits of D14 and R15 indicates whether D14 is to be subtracted from, or added to, R15 to form R14. The D14 and R14 sign bits are then compared to determine the Q14 value. At the end of the last iteration (where $N = 0$), the resulting R0 value is the final 16-bit remainder that results when dividing one number by another.

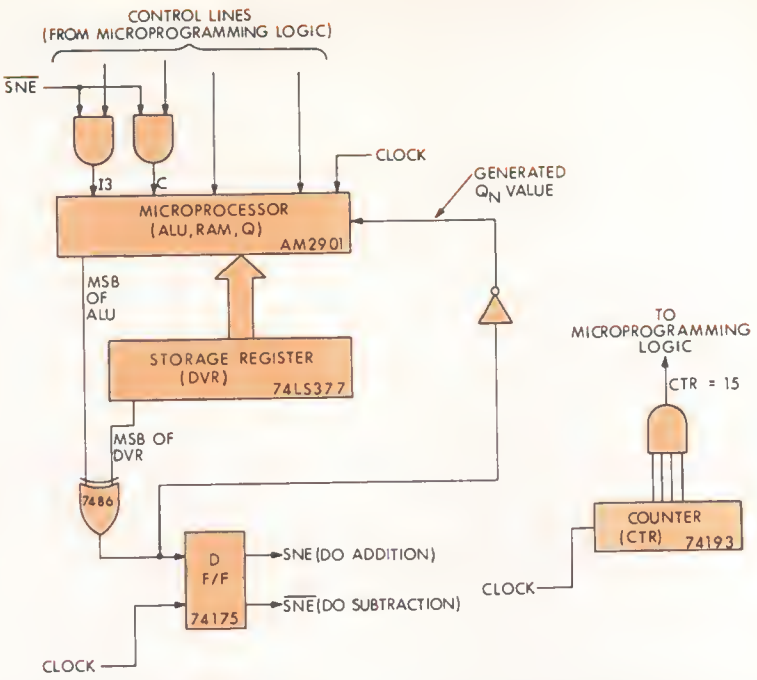


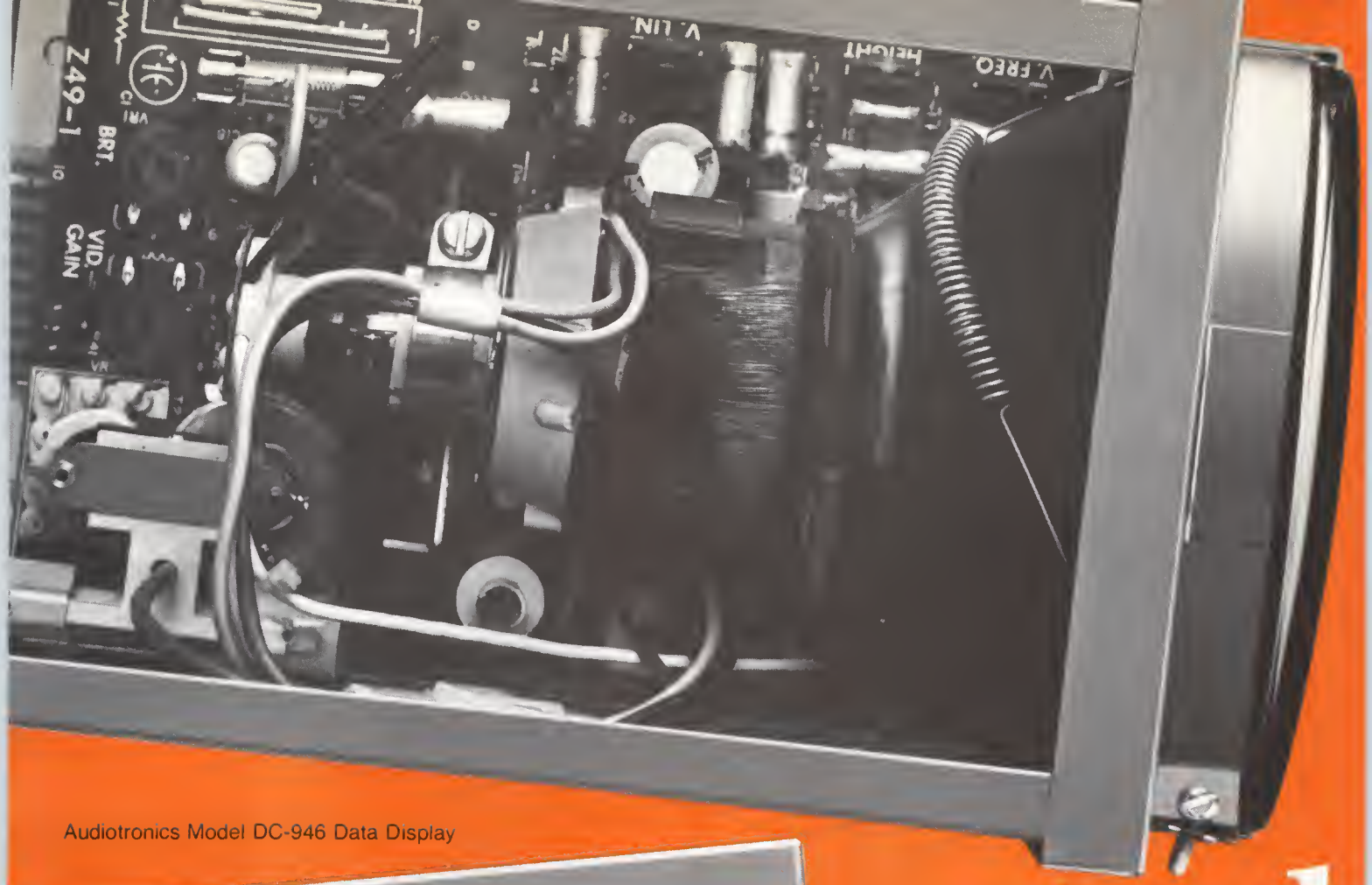
Fig 1 Hardware implementation of division algorithm. Most significant bits of ALU and DVR determine both QN value and next arithmetic operation. Present arithmetic operation is determined by previous condition of ALU and DVR sign bits, which is stored in SNE. CTR output determines next microinstruction address

Implementing the Division Algorithm

A block diagram of the hardware configuration used in implementing the division algorithm is shown in Fig 1. A 4-bit iteration counter (CTR) counts the number of divide iterations. Two 8-bit 74LS377 registers (DVR) store the 16-bit divisor. Four 4-bit slice Am2901 microprocessors[2] store the 32-bit dividend, perform the arithmetic add/subtract operations, and store the resulting quotient and remainder.

The most significant half of the dividend is stored in one of the microprocessor's 16 general purpose random access memory (RAM) registers, and the least significant half of the dividend is stored in the microprocessor's Q register. In implementing the division algorithm, the divisor value stored in DVR remains fixed and is added to, or subtracted from, the most significant half of the dividend. Thus, for the first iteration, the highest multiple of the divisor ($D \times 2^{15}$) is subtracted from, or added to, the dividend. Then, during subsequent iterations, the complete dividend in the RAM and Q registers is shifted left, thereby enabling decreasing multiples of the divisor to be subtracted from, or added to, the successively generated remainder values ie, R15 to R0). Furthermore, the quotient bit generated during each iteration is stored in the least significant bit position of the Q register as the dividend is shifted left. Thus, at the end of 16 iterations, the Q register contains the 16-bit quotient, and the RAM register contains the 16-bit remainder (R0).

The microprocessor executes a complete divide iteration in only one microinstruction by performing an arithmetic operation and writing the shifted results of that operation back into a RAM register at the end of the same microinstruction. Therefore, during the execution of a single microinstruction, a new remainder (R_N) is generated and is shifted left one bit to prepare for the next iteration. In the arithmetic operation that takes place during the microinstruction, the divisor is subtracted from R_{N+1} to form R_N, provided that the R_{N+1} and divisor signs are the same; otherwise, the divisor is added to R_{N+1}. The sign of R_{N+1} is the most significant bit of the arithmetic process that took place during the previous microinstruction. At the end of each microinstruction time, this sign bit is compared with the divisor sign bit held in DVR, and a sign-not-equal (SNE) flipflop is set or reset according to the results of the comparison. The control lines that define the microprocessor arith-



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metic operations are set up to indicate that a subtraction is to take place during a divide iteration if SNE is false; when SNE is true, the control lines are changed to produce the required add operation. In practice, this involves using two AND gates (Fig 1) to change the inputs going to the microprocessor's I3 and C lines from a 1 to a 0.

The hardware in Fig 1 is controlled by the microinstructions[3] in the divide microprogram. The iterative portion of the divide microprogram is shown in Fig 2, where each box in the flowchart represents one microinstruction. At the end of the first microinstruction, the SNE flipflop is set or reset according to the sign of the dividend and the divisor; the dividend is initially shifted left one bit to generate the equivalent of the $D15 = D \times 2^{15}$ condition, and CTR is set to 0.

During the second microinstruction, the first modified dividend (R15) is generated by either subtracting or adding the divisor from or to the most significant half of the dividend—depending upon the SNE condition determined at the end of the first microinstruction. At the end of the second microinstruction, five events take place: a new SNE condition is once again determined by the R15 and divisor sign bits; the R15 value is loaded into RAM; the RAM and Q registers are shifted left to generate the equivalent $D14 = D \times 2^{14}$ condition for the next iteration; the Q15 value, generated according to the sign bits of R15 and the divisor in DVR, is shifted into the least significant bit position of the Q register; and CTR is incremented.

This second microinstruction is executed a total of 15 times in order to generate the Q15 to Q1 values. The Q0 value is generated in the third microinstruction (Fig 2). In generating the Q0 bit, the nonshifted result (ie, $R0 = R1 \pm D0$) is the final remainder. However, the Q register must be left-shifted to receive the Q0 bit. Since the microprocessor cannot shift the Q register contents without also shifting the RAM register contents, a RAM and Q register shift must be performed. During this shift, the most significant R0 bit is temporarily shifted into the least significant bit position of the RAM register as Q0 is shifted into the least significant bit position of the Q register. At the end of the last microinstruction (Fig 2), this bit is right-shifted back into the most significant bit position of the RAM register.

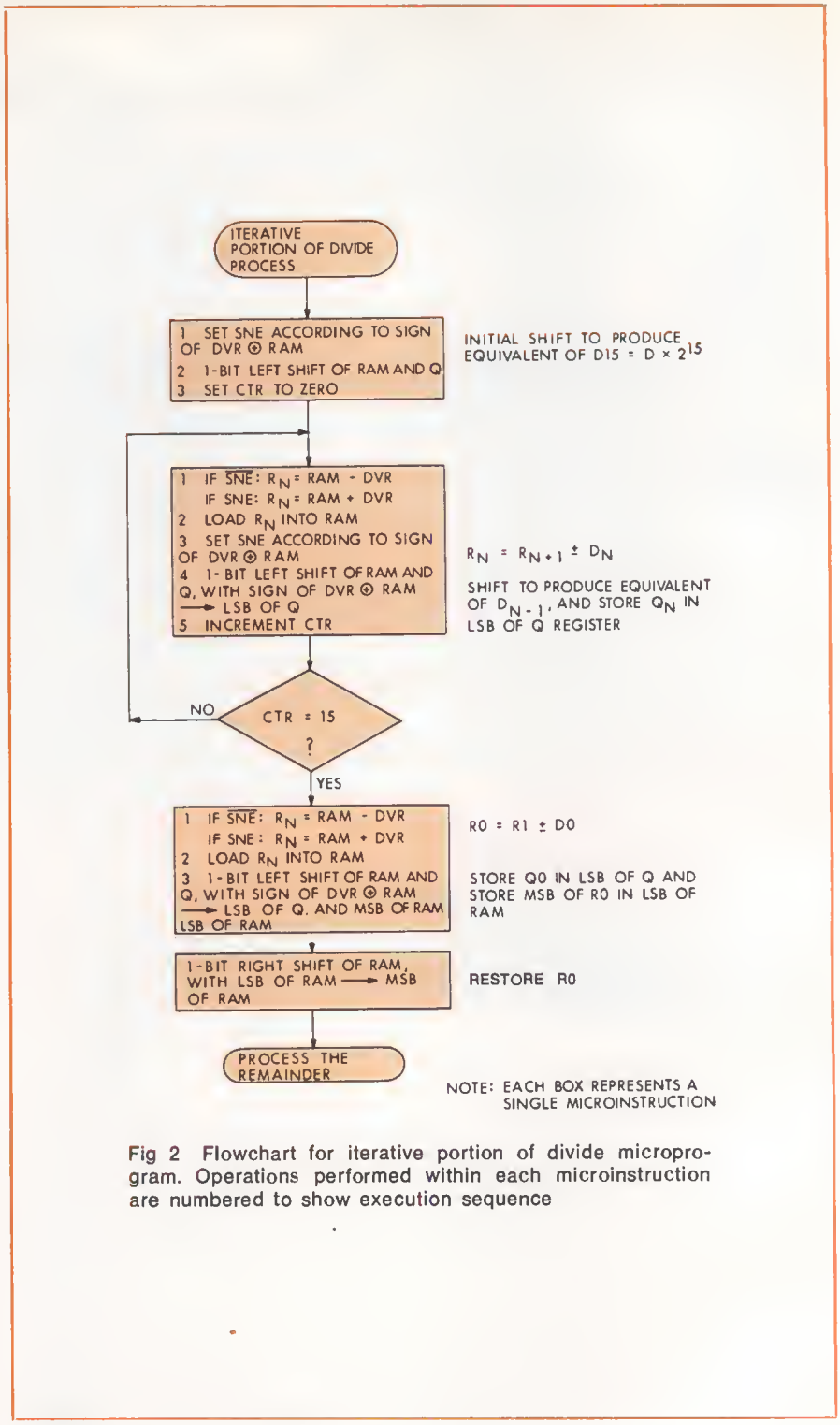

Fig 2 Flowchart for iterative portion of divide microprogram. Operations performed within each microinstruction are numbered to show execution sequence

Division Example

An example of the divide iteration process is given in the Table. For simplification, 4-bit binary numbers rather than 16-bit numbers are used. In the Table, the register contents are shown at the beginning of the microinstruction. At this time, the output of the microprocessor arithmetic logic unit (ALU) contains the results of the $R_N = R_{N+1} \pm D_N$ arithmetic operation. The results of the operations taking place at the end of a microinstruction are shown during the next microinstruction. Thus, the new SNE value, the value of the quotient bit to be shifted into the

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Division Process Example for Nonrestoring Divide Algorithm

		26	÷	6	=	4	+ 2
		00011010	÷	0110	=	0100	+ 0010
		(Dividend)	÷	(Divisor)	=	(Quotient)	+ (Remainder)
Step	DVR	ALU	RAM	Q	CTR	SNE	COMMENTS
1	0110	—	0001	1010	—	—	Divisor, dividend, and counter loaded
2	0110	0001	0001	1010	0	—	Initial shift
3	0110	1101	0011	010X	0	0	Subtract and shift
4	0110	0000	1010	10X0	1	1	Add and shift
5	0110	1011	0001	0X01	2	0	Subtract and shift
6	0110	1100	0110	X010	3	1	Add and shift (last iteration)
7	0110	—	1001	0100	—	—	RAM right shift
8	0110	—	1100	0100	—	—	End

Note: Table shows all pertinent outputs at the beginning of each microinstruction

least significant bit position of Q, and the contents of the RAM register are all determined by the ALU and DVR values given in the previous iteration. For example, the results of the add and shift that take place at the end of Step 6 (see the Table) are given in Step 7. In the Table, the bit shifted into the least significant bit position of Q during the initial shift in Step 2 is not part of the quotient and, therefore, is indicated by an X in Steps 3 to 6. Step 8 contains the quotient value in the Q register and the remainder in the RAM register. Note that the remainder is the negative decimal value −4 rather than the positive decimal value 2, as indicated in the equation above the table. The −4 remainder is corrected in the third part of the divide process by adding the value of the divisor to the remainder held in the RAM register.

Summary

By performing all required iteration operations in one microinstruction, division iteration time can be cut in half. All iteration operations are performed by using hardware to determine the required arithmetic operation, and by shifting the arithmetic results at the end of the microinstruction. In implementing the division algorithm, the microprocessor holds the dividend, performs the arithmetic operations, and shifts the arithmetic results; a storage register holds the divisor; and a counter determines the address of the next microinstruction to be executed. In many applications, microprocessor, storage register, and counter are already present in the system for the execution of other microprograms. Therefore, only a minimal amount of decisional hardware needs to be added to implement the division algorithm. If a microprocessor is not present, a 32-bit shift register can be used to hold the dividend, and an arithmetic unit can perform the add/subtract operations.

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1. E. L. Braun, *Digital Computer Design*, Academic Press, 1963
2. Advanced Micro Devices, *Am2901, Am2909 Technical Data Manual*, Advanced Micro Devices, Inc, Sunnyvale, Calif, 1978
3. J. C. Conway, "Hardware Approaches to Microprogramming with Bipolar Microprocessors," *Computer Design*, Aug 1978, pp 83-91

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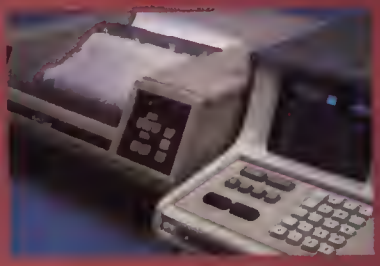

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CIRCLE 59 ON INQUIRY CARD

TECH NOTE

Improving Memory Reliability Through Error Correction

An analytical method evaluates enhancement in memory reliability with single-error correction. For a simple memory card organization, decreases in card replacement and rates of replacement are calculated

A. V. Ferris-Prabhu IBM General Technology Division, Essex Junction, Vermont

Reliability of semiconductor components in memory technology has increased phenomenally; failure rates of 0.01% per 1000 power-on hours, or lower, are not unusual. However, both device density and memory capacity have also increased by orders of magnitude. Therefore, to achieve and maintain superior reliability, more attention may need to be given to the use of error correction codes to mask failures.[1,2,3]

Memory Organization

Consider a simple single-card memory that contains in addition to several support chips, 16 memory chips. Each of these has eight word lines and eight bit lines for a 64-bit capacity. Each chip is addressed during each data transfer, and delivers one bit to the same position in a 16-bit data word. A 1024-bit (ie, 1k) memory card, as described, can deliver 64 16-bit words. With this memory organization, even if an entire chip fails, only one defective bit is delivered per data word. However, there will be a bad bit in each of 64 different 16-bit words.

If there is no error correction capability, the delivery of even a single faulty bit leads to a card failure. If there is single-bit error correction, however, up to one defective bit can be delivered at each data transfer without resulting in card failure. Thus, for this memory card to survive with no error correction, all 16 memory chips must survive. To understand the essence of the effect that error correction has on reliability, two simplifying assumptions are made: first, the effect of support chip failures is neglected; and second, of all the failure modes that contribute to memory chip failure, those modes that result in the entire chip failing (ie, chip kills) are dominant.

The effect of the first assumption is to decrease the memory failure rate by a known and usually constant value that is easy to compute. Support chip failures are not usually error correctable; hence, neglecting them does not affect this discussion. The effect of the second assumption is to increase the memory failure rate. This latter assumption makes it unnecessary to consider calculation complexities that result from fail-

ures of single cells, bit lines, or word lines. Such failures also result in the delivery of one or more bad bits, but not to as many words. Consequently, an assumption of this kind, which is frequently made,[2] gives a worst-case conservative boundary on memory reliability. The analysis is considerably simplified, and results in insignificant error if the chip kill failure mode contribution to the chip failure rate is greater than about 75% to 80%, as is frequently the case.

Survival Probability

For a large number of such single-card memory systems, let S(t) denote the cumulative fraction of cards surviving at any time t. For S, the subscript 0 denotes the case of no error correction, and the subscript 1 denotes the case of single-error correction. Let s(t) denote the cumulative fraction of all 16 chips surviving at any time t. Then, with no error correction

$$S_0(t) = (s[t])^{16}. \quad (1)$$

However, if there is single error correction, up to one chip may fail and

$$S_1(t) = (s[t]^{16} + 16\,(s[t]^{15} \times (1-s[t]) \quad (2)$$

where the second term on the right shows the increase in the fraction of cards surviving because only 15 chips need to be good. Eq (2) can also be written as

$$S_1(t) = S_0(t)\left[1 + N\left(\frac{1}{s(t)} - 1\right)\right] \quad (3)$$

where, for generality, the number 16 has been replaced by N. In Eq (3), s(t) has a value between 0 and 1. Therefore, the quantity

$$\left(\frac{1}{s(t)} - 1\right)$$

can never be negative. Thus, the reliability improvement factor

$$\left[1 + N\left(\frac{1}{s(t)} - 1\right)\right]$$

must be equal to or greater than 1. As expected, the effect of single-bit error correction is to improve reliability. Initially, the cumulative fraction of chips surviving is very close to 1, and the improvement in card reliability due to error correction is small. But as time passes and the cumulative fraction, s(t), of chips surviving becomes smaller, the improvement due to error correction becomes larger. However, when the number of chips that fail cause more than one bad bit to be delivered to a word, the memory card will fail, as single-error correction cannot mask more than one bad bit per word.

Replacements Needed

The preceding explanation has developed expressions for the cumulative fraction of chip survivors. However, in reliability work, it is necessary to know the total number of replacements that will be needed during the operational life of a high component density system and the rate at which replacements will be needed. The first quantity answers the question, "How many?"; the second answers the question, "When?" It is necessary to know both in order to determine suitable manufacturing, servicing, and pricing strategies. These questions are answered by relating the number of replacements to the cumulative fraction of survivors.[4] Consequently, it is helpful to make another simplifying assumption: chip failures are governed by a Poisson process, where the occurrence of an event is independent of the occurrence of previous events. Although such an assumption is not strictly correct, experience shows that it can often be used with great saving in calculational effort and at a very small sacrifice in accuracy. For such a process, the number of replacements is given by the term

$$H(t) = -\ln S(t) \quad (4)$$

where ln stands for the logarithm to the base e. In reliability work, H(t) is called the cumulative hazard function. It is equal to the number of replacements needed only for exponential distributions that are characteristic of a Poisson process. For all other distributions, the number of replacements needed is given by a more complicated expression.[5] Eqs (1) and (3) show that with no error correction

$$H_0(t) = -\ln S_0(t) \quad (5)$$

and with single-error correction

$$H_1(t) = H_0(t) - H_c(t) \quad (6)$$

where

$$H_c(t) = \ln\left[1 + N\left(\frac{1}{s(t)} - 1\right)\right]. \quad (7)$$

As S_0 (t), the cumulative fraction of cards surviving, is always less than or equal to 1, its natural logarithm is negative; therefore, the number of replacements (H_0) is a positive number. Also, as shown earlier, the quantity

$$\left[1 + N\left(\frac{1}{s(t)} - 1\right)\right]$$

is never less than 1; thus, its logarithm is never negative. Hence, H_c (t) is either zero or positive. The effect of error correction is to decrease, by $H_c(t)$, the number of replacements, $H_0(t)$, that would be needed if there were no error correction.[6] It is assumed for simplicity in this discussion that failed cards are not repaired and reused. If cards are repaired and reused, the number of cards that need to be repaired does not change with error correction, but the time interval between repairs is increased. The assumption of a Poisson process for chip failures means that a constant chip failure rate (λ) has been assumed. Thus,

$$s(t) = e^{-\lambda t} \quad (8)$$

then

$$H_0(t) = \ln(e^{-\lambda t})^N = N\lambda t \quad (9)$$

and

$$H_1(t) = N\lambda t - \ln(1 + N[e^{\lambda t} - 1]) \quad (10)$$

For large values of time

$$H_1(t) \simeq (N-1)\lambda t - \ln N \quad (11)$$

As the argument of the logarithm is never less than 1, the effect of error correction is to decrease the number of replacements needed.

The instantaneous failure rate, h(t), which for a Poisson process is the same as the replacement rate, also changes when there is error correction.

With the definition

$h(t) = dH(t)/dt$,

$$h_0(t) = N\lambda \quad (12)$$

and

$$h_1(t) = N\lambda\,[1 - 1/(N - [N-1]e^{-\lambda t})] = h_0\,[1 - 1/(N - [N-1]e^{-\lambda t})] \quad (13)$$

At $t = 0$

$$N - (N-1)e^{-\lambda t} = 1 \quad (14)$$

Thus, there is initially no difference in the replacement rate whether or not there is error correction. This, of course, is as expected.

For very large values of time, the term $e^{-\lambda t}$ essentially vanishes, and the correction term becomes $(1 - 1/N)$.

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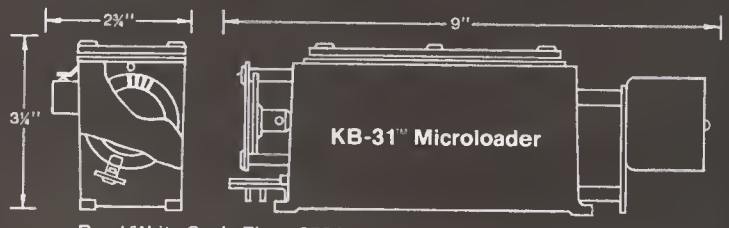

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At no time is the correction term larger than unity. As time progresses, the effect of error correction is to slow down the replacement rate until eventually it becomes constant at the value $(n - 1)$.

Numerical Results

The derived equations have been computed for $N = 16$ and for $\lambda = 0.1\%/kh$ and $\lambda = 0.01\%/kh$. The results for $\lambda = 0.1\%/kh$ are plotted in Fig 1, showing the distinct increase in the fraction of survivors due to single-error correction. The percentage of the original number of cards in the field that will need to be replaced by time t has also been computed, with and without error correction. With $\lambda = 0.1\%/kh$, it takes 10,000 power-on hours before 1% of the cards need be replaced when there is single-error correction, whereas without error correction, at that time, 16% of the cards would need to be replaced.

At the lower chip failure rate of $\lambda = 0.01\%/kh$, the effect of error correction is not so dramatic. The improvement at 10,000 h due to single-error correction is now only about 1.6%. However, if there are 10,000 cards in the field, decreasing the number of replacements by 160 is not inconsequential, not only in terms of money saved by the manufacturer, but also of inconvenience avoided by the user. This dramatic improvement is shown in Fig 2, where the crosshatched region indicates the savings obtained in the number of replacements.

The rate of replacement for both failure rates is depicted in Fig 3. Without error correction, the rate at which replacements are needed is constant. With error correction, the replacement rate does rise fairly rapidly; however, it is always lower than the rate would be without error correction, and it stabilizes to a constant value of $(N - 1)/N$ times the replacement rate with no error correction. In all these results, the effect of support chips failing has been neglected since they are usually not error correctable. If included, the effect would be merely to raise the card replacement—and replacement rate—values by an amount equal to the failure rate of the support chips times the number of such chips.

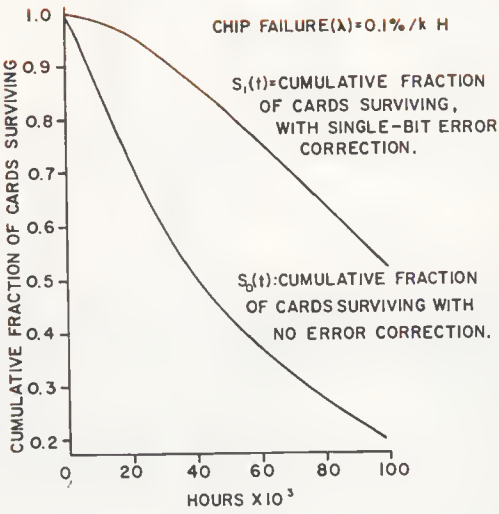

Fig 1 Cumulative fraction of cards surviving without and with single-bit error correction. Significant increase in cumulative fraction of cards surviving results when single-bit error correction is used

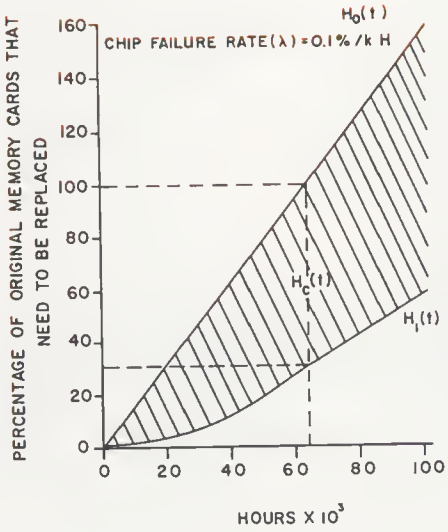

Fig 2 Percentage of original memory card population that needs to be replaced, without (upper curve) and with (lower curve) single-error correction. Difference between two curves represents percentage of card replacements saved due to single-error correction. Notice that by about 65,000 h, without error correction, each original card needs to be replaced once, whereas with single-error correction slightly over 30% of original cards need be replaced by this time

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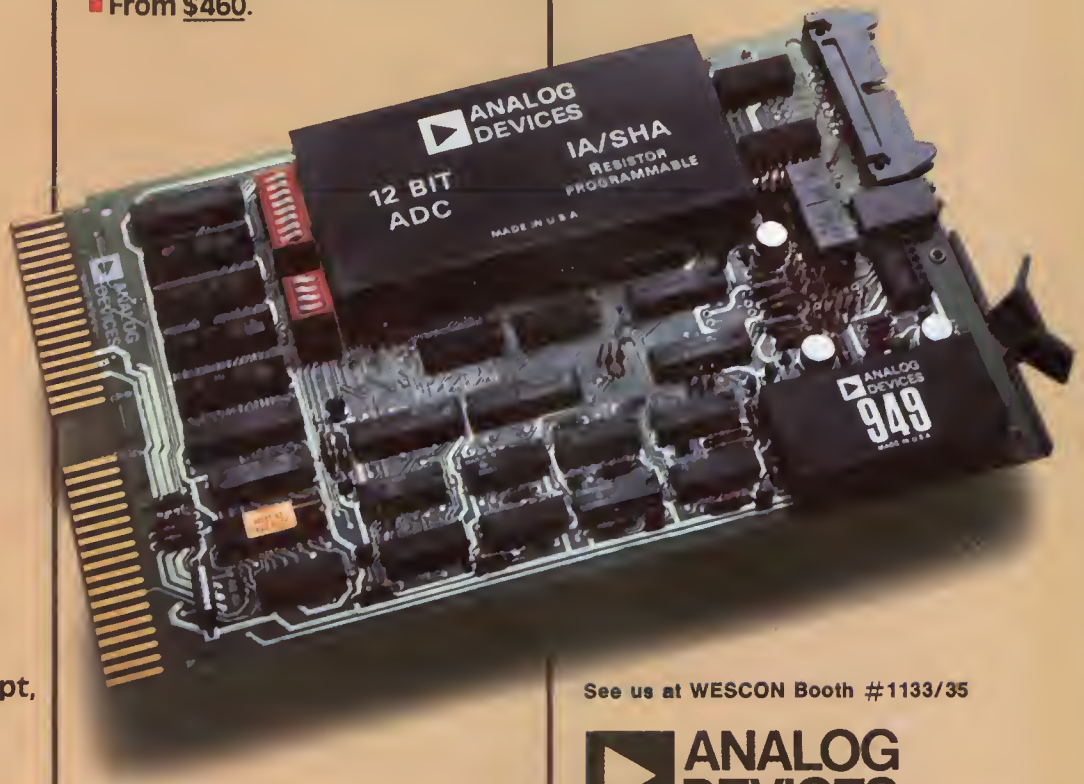

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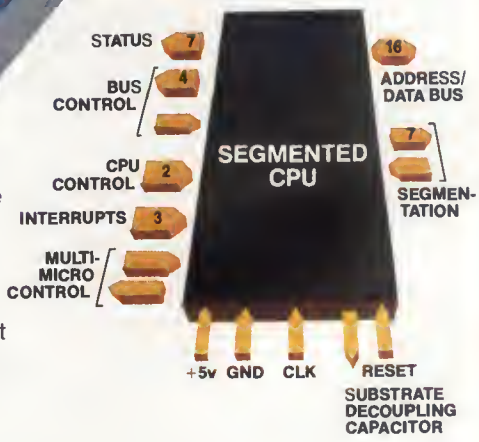

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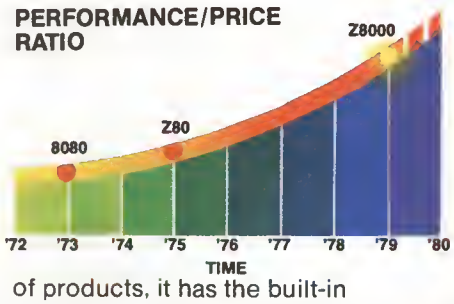

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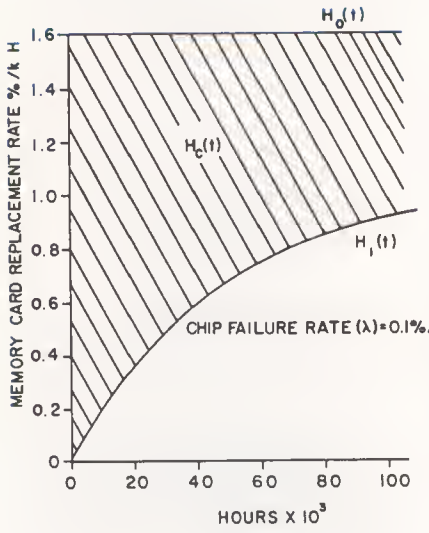

Fig 3 Replacement rate, without (upper curve) and with (lower curve) single-error correction. Rate is constant (with no error correction) because of assumption of a Poisson process governing chip failure rate and increases from zero to a constant value with single-error correction. Difference between two curves is decrease in replacement rate due to single-error correction. Decrease becomes less as time progresses, tending to a constant value

Conclusions

As this discussion reveals, the use of single-error correction has a noticeable effect in improving reliability. If the individual chip failure rate (λ) is small, and the number of error correctable components (N) is small, the effect of error correction may not be significant. But, even if N is not large, and if the total number of systems (1-card memories in this example) in the field is large, a considerable saving can be obtained in terms of the number of replacements needed. This saving can be much greater than the cost of the hardware required to perform single-error correction (and double-error detection) if the volume of the product is sufficiently large.

Many factors, such as field service and stocking costs, enter into the computation of the break-even volume, but they are beyond the scope of this discussion. However, even if the volume of product is small, there are situations, such as onboard control of interplanetary vehicles, where extremely high reliability is needed over periods of several months and even years. In such cases, the use of single-error correction can improve the reliability by several orders of magnitude. Thus, it is becoming more necessary to utilize error correction in a wider range of products than has been previously the case.

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5. J. C. McCall, "Renewal Theory—predicting product failure and replacement," *Machine Design*, March 26, 1976, pp 149-154
6. A. V. Ferris-Prabhu and N. D. Lubart, "Reliability Analysis for Simple Systems," *Microelectronics and Reliability*, Vol 15 1976, pp 555-560

TECH BRIEF

Secure Communications System

A potentially inexpensive, hardware coded digital message encoder is almost unbreakable

An encoding/decoding system for secure communications employs an electronically randomized variant of quadraphase modulation and demodulation between two synchronized transceivers. The coding method has random properties that make it difficult to decipher. Constructed from off-the-shelf components, the system is inexpensive as well as secure.

A typical transceiver for the encoder/decoder comprises a master timer, a message encoder and transmitter, and a message decoder and receiver. Messages are encoded by using the combined outputs of two pseudorandom sequence generators as shown in Fig 1. These are 41-stage shift register devices, and the particular sequence obtained from each depends on which taps are used. With a clock rate of 250 kHz, a maximum-length sequence takes 102 days to repeat. Each sequence generator produces a different sequence, with a different length. These are combined in a modulo-two adder to form a new code, which is used to encode the transmitted data. Encoded data, along with one of the original pseudorandom sequences, are transmitted via quadraphased modulation or other suitable technique.

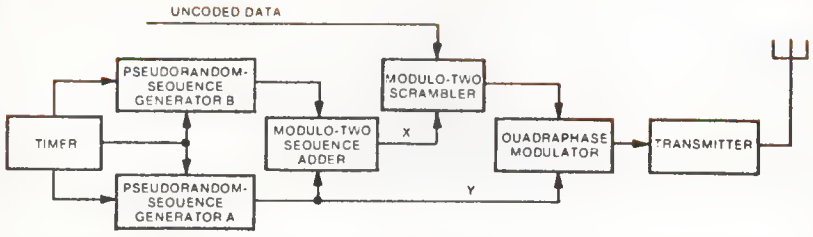

Fig 1 Encoder/transmitter is controlled by timer that uses stable quartz-crystal oscillator as reference. Shift registers placed at points X and Y provide delays that match those in receiver/decoder

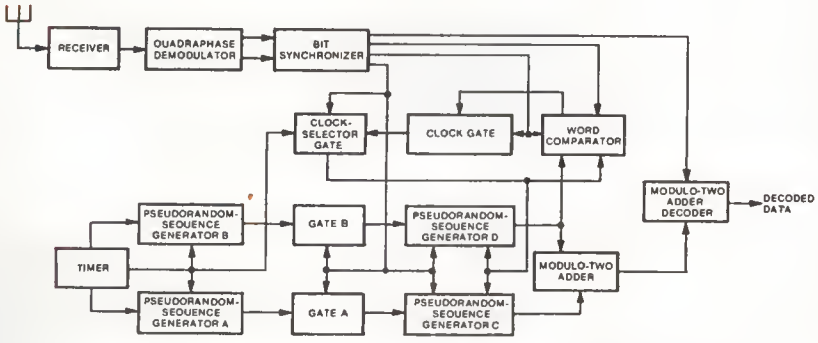

Fig 2 Receiver/decoder is controlled by a timer set identically to that in transmitter/encoder, and uses identical shift registers

The timer is used to synchronize the encoding and decoding for the transmitter and receiver. Both generated sequences are reset periodically and at slightly different times. At the receiver, the actual pin assignments for shift register outputs and the program that is used to change tap assignments must be known.

The receiver/decoder is shown in Fig 2. The decoder produces the same two pseudorandom sequences as the transmitter/encoder. These are used to reproduce the encoding sequence, and the pseudorandom sequence that was transmitted with the encoded data is used in the receiver for synchronization. A pair of sequence generators identical to the first act as shift registers when no message is being received. When a message is being received, the first pair of sequence generators (A and B) continues to produce the timed coding sequence; the second pair (C and D) is used to decode the received signal.

Before this system is initialized, timers at all stations must be synchronized, which is done by using a reference timer. Finally, the coding parameters must be set in by switches or using magnetic cards.

Note

This work was done by George D. Doland of Lockheed Electronics Co, Inc, for Johnson Space Center. For further information, write to: John T. Wheeler, Johnson Space Center, Code AT3, Houston, TX 77058.

Patent Status

Inquiries concerning rights for the commercial use of this invention should be addressed to: Marvin F. Matthews, Lyndon B. Johnson Space Center, Mail Code: AM, Houston, TX 77058. Refer to MSC-16462.

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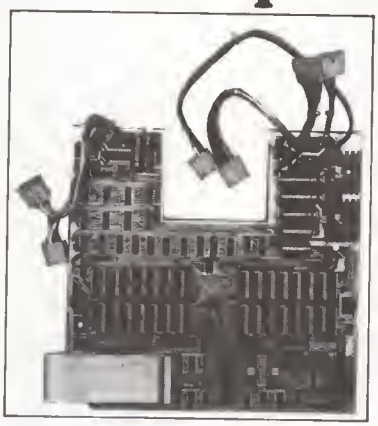

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CIRCLE 65 ON INQUIRY CARD

APPLICATION BRIEF

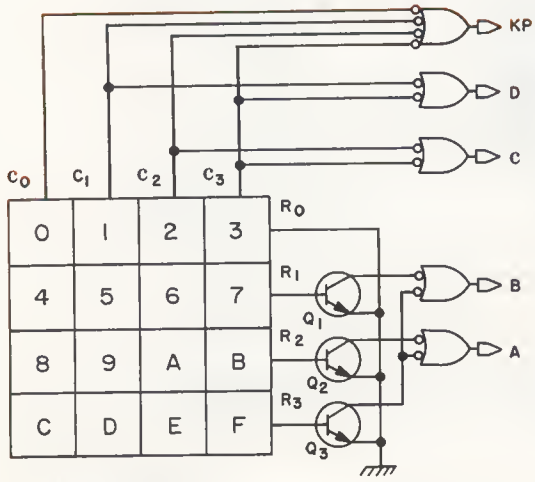
TTL Circuit Encodes Multiplexed Keyboards Without Strobes

A 4 x 4 TTL circuit encodes multiplexed keyboards without clocks, counters, latches, or strobes

Donald E. Brodnick

University of Illinois, Urbana-Champaign, Illinois

A simple circuit design allows multiplexed keyboards to be encoded with few components. The Figure shows a 4 x 4 keyboard encoder circuit that requires only one 7400 quad 2-input NAND gate package, one-half of a 7420 dual 4-input NAND gate package, and three type 2N2222 discrete transistors. The encoder generates a 4-bit code (ABCD) and a key pressed (KP) flag. The circuit uses only combinational logic and requires no memory of previous states as with common strobed encoders. Although this design eliminates any multiple key rollover capability, it also eliminates clocks, counters, latches, and strobes. The code produced for multiple key closures is the OR combination of each code for each key pressed. The complete code is available approximately one gate delay after any key is closed. The entire circuit for the 4 x 4 encoder could be integrated into one 16-pin package using small scale integration. Medium scale integration could produce a 16-column by 4-row encoder in a 28-pin package.



Multiplexed keyboard encoder circuit. Three transistors convert current drawn from column line encoder gate inputs into current drawn from row line encoder gate inputs. Four 2-input NAND gates encode key position in 4-bit word (ABCD). One 4-input NAND gate tests for any column line grounded and generates key pressed (KP) signal

The Figure explains circuit operation. C_0 through C_3 are the column lines of the keyboard; R_0 through R_3 are the row lines. Outputs A, B, C, and D form the 4-bit key code. The KP output indicates both "key pressed" and "code valid" when high. With no key pressed, all the transistor-transistor logic (TTL) inputs connected to the column lines float to logic 1 (high). The C and D outputs of the column decoder gates, as well as the KP output, are low. Transistors Q_1, Q_2, and Q_3 are all cut off by the absence of any base currents. Therefore, all the TTL inputs of the row encoder gates are high and the A and B outputs are low.

When a key is pressed in row 0, one of the column lines is grounded. The column position is encoded on outputs C and D. Row outputs A and B remain low, but output KP goes high. When a key is pressed in any other row, one of the column lines is pulled low by the base-emitter junction of the transistor connected to that row. That transistor's collector grounds one or more of the row encoder inputs. Row position is encoded on A and B. Outputs C, D, and KP are encoded as for row 0.

Although this circuit design functions adequately, open-circuit logic 1s at TTL inputs may be unacceptable in certain applications. Thus, pullup resistors may be connected to column lines and transistor collectors to restore normal logic levels and improve noise immunity.

For some applications, the outputs need to be debounced. Almost any debouncing scheme may be applied to this circuit. The KP flag may be filtered and delayed by hardware. In a microprocessor application, a software delay may be inserted between KP flag recognition and key code acquisition.

Larger keyboards can easily be encoded. Two 2-input NAND gates, one 16- to 4-line encoder, and three discrete transistors will encode a 16 x 4 multiplexed keyboard. The 16- to 4-line encoder can be made from four 7430 8-input NAND gates. By adding another discrete transistor and a 4-input NAND gate, the KP flag may be obtained by testing the four row-line transistor collectors. □

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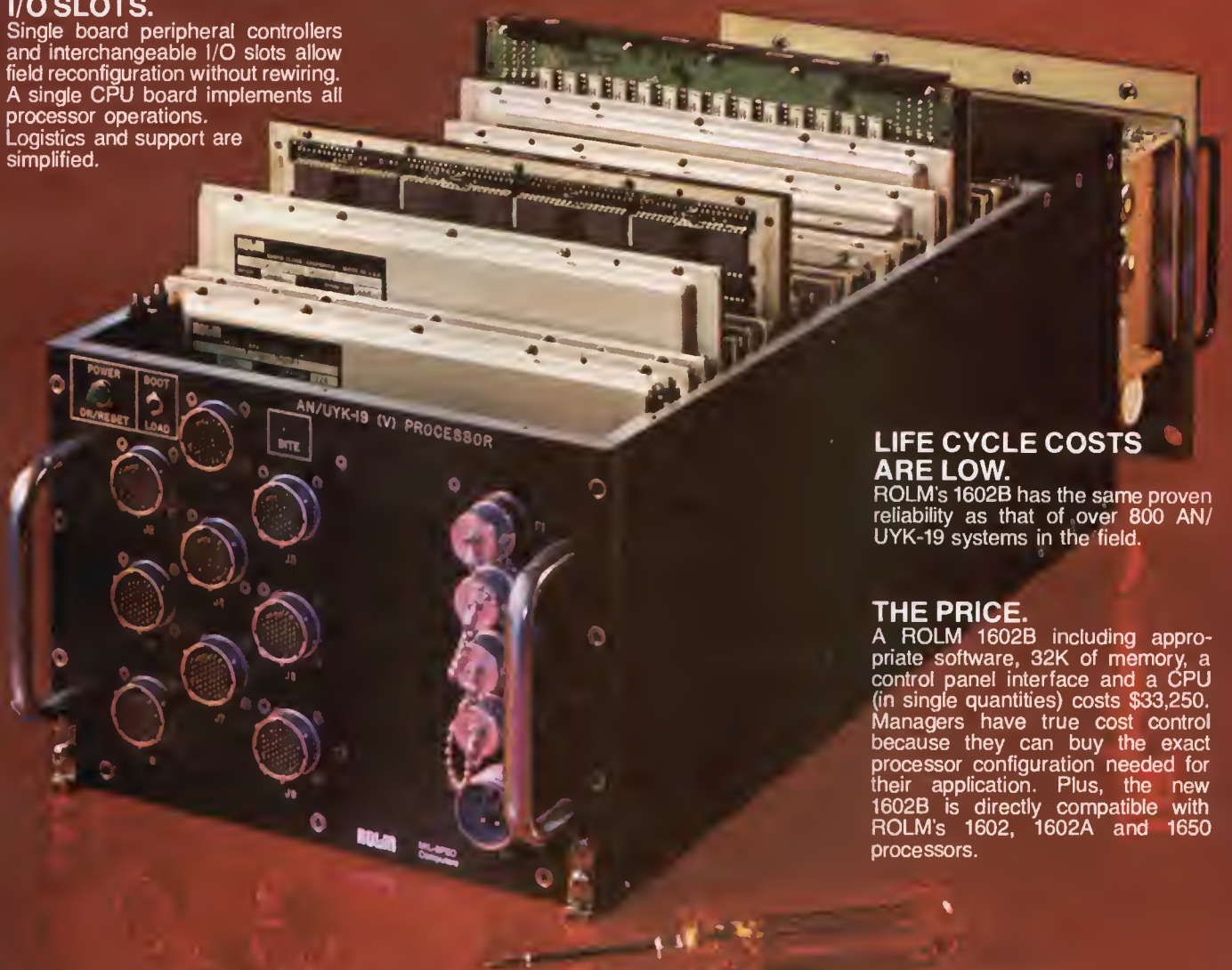

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CIRCLE 66 ON INQUIRY CARD

INTERFACING FUNDAMENTALS: SORTING

David G. Larsen and Peter R. Rony
Virginia Polytechnic Institute and State University
Christopher A. Titus and Jonathan A. Titus
Tychon, Inc

Quite often a program will execute much faster if the values it accesses are sorted. Sorting, or the rearrangement of data values in a list, table, record, or file in an ascending or descending order, is also useful when data or alphanumeric strings have to be output to a printer or cathode ray tube in a specific order. Data sorting methods include straight insertion sort, binary insertion sort, Shell's sort, bubble sort, quick sort, heap sort, merge-exchange sort, and 2-way merge sort. In general, all of these can be classified as an insertion, exchange, selection, merge, or distribution method.[1,2] This discussion will cover only the exchange method of sorting numeric values, specifically, the bubble sort method. Although it is one of the slowest methods, it is probably the easiest subroutine to write.

A list of five 8-bit unsigned data values (nodes), as shown in Table 1, is stored in memory from memory location X to memory location X + 4. This example sorts the list in ascending order, storing the smallest value in X and the largest in X + 4. If the data value in memory location X is greater than the data value in location X + 1, the two values are exchanged. This means that the data value in location X is written into X + 1, and the value previously stored in X + 1 is stored in location X. A register or memory location is loaded with a specific value to indicate that an exchange has taken place. If the data value in location X is less than the data value in X + 1, no exchange takes place.

Regardless of whether or not an exchange occurs, the microcomputer next compares the data values in memory locations X + 1 and X + 2. If the content of location X + 1 is greater than X + 2, an exchange takes place; if the content of memory location X + 1 is less than the content of memory location X + 2, no exchange takes place. This compare and exchange process continues until the microcomputer reaches the end of the list. At this point, the microcomputer examines the content of a register or memory location to see if any exchanges took place. If any did, the microcomputer passes through the list again. Only when the microcomputer makes a pass through the entire list, and no exchanges take place, is the list sorted.

The first pass through the list in Table 1 exchanges the 3 and the 2. The 5 and 4 are also exchanged, followed by the 5 and 1. On the second pass, the 4 is bubbled up to memory location X + 3, just behind the 5. The 3 and 2 are moved to their appropriate positions in the list in the third and fourth passes. On the fifth pass, the data values are in the proper sequence, so no exchanges occur; therefore, the list is sorted. A bubble sort subroutine for the 8080 microprocessor, which sorts 8-bit unsigned numbers, is listed in Table 2.

The BSORT subroutine must be called with the starting address of the list in register pair H and the final address of the list in register pair D. If the list in Table 1 were sorted by the BSORT subroutine, register pair H would contain address X and register pair D would contain X + 4. Starting at BSORT, the microprocessor subtracts the starting address (X) from the final address

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Feature \ Printer	Integral Data 440	Tally 1200	Lear-Seigler 300	Texas Instruments 810	Centronics 779-2
96-character ASCII set, upper and lower case	YES	OPTION	YES	OPTION	NO
Software-selectable character sizes	YES	NO	NO	OPTION	NO
Throughput, lines per minute @ 10 char./line @ 132 char./line	275 42	100 40	Data not available	440 64	130 21
Parallel and RS-232 serial interfaces standard	YES	NO	NO	NO	NO
CRT screen buffer	OPTION	NO	OPTION	NO	NO
Footprint (W x D = sq. ft.)	1.37	3.45	3.18	3.58	2.44
Weight (lbs.)	20	64	50	55	45
Forms length control	YES	OPTION	YES	OPTION	NO
Full dot plotting graphics	OPTION	NO	NO	NO	NO
Unit Price	$995	$2500	$1995	$1895	$1350

Comparison data from manufacturers' current literature

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CIRCLE 67 ON INQUIRY CARD

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TABLE 1

Bubble Sorting a Data List

Memory Address	Initially	1st Pass	2nd Pass	3rd Pass	4th Pass	5th Pass
X	3	3	2	2	2	1
X+1	2	2	3	3	1	2
X+2	5	5	4	1	3	3
X+3	4	4	1	4	4	4
X+4	1	1	5	5	5	5
		Result	Result	Result	Result	Result
		2	2	2	1	1
		3	3	1	2	2
		4	1	3	3	3
		1	4	4	4	4
		5	5	5	5	5

(X + 4) and saves the result (the node count) in register pair D. The node count indicates to the microprocessor when it has reached the end of the list. At PASS1, the starting address of the list (X) and the node count are saved on the stack. Register C is loaded with 000, since it will be used as the "exchange indicator." If an exchange takes place during a pass through the list, register C will be set to 377. This means that once the microprocessor has examined all of the nodes in the list, it will examine the content of register C to determine if any exchanges took place during the last pass through the list. If register C contains 377, at least one exchange took place, so the microprocessor will have to make another pass through the list.

The actual compare and exchange instructions begin at UP1. The first node is moved to register A, and the memory address in register pair H is incremented by one to X + 1. The 2 in memory location X + 1 is compared to the 3 in register A. If the content of X + 1 is equal to or greater than the content of register A, the microprocessor jumps to NEXT. This means that no exchange should occur.

If the content of memory (2) is less than the content of register A (3), the node in memory is moved to register B and the content of register A is stored in memory. The memory address is then decremented (X + 1 to X) and the node in the B register (2) is written back into memory. The memory address is then incremented (to X + 1). Since an exchange just took place, register C is loaded with 377.

By decrementing the node count in register pair D, the microprocessor can determine if the entire list has been examined. If it has not, the microprocessor jumps back to UP1, where the 3 in X + 1 is compared to the 5 in X + 2. As expected, these two nodes are not exchanged. The next time through the UP1 loop, the microprocessor compares and exchanges the 5 in X + 2 with the 4 in X + 3. The next execution compares and exchanges the 5 in X + 3 with the 1 in X + 4. At this point, the node count in register pair D is decremented to zero.

Because of this, the microprocessor examines the content of register C. If the content is not 0 (377), the microprocessor jumps back to PASS1 so that it can make another pass through the list. The microprocessor continues to make passes through the list until register C contains 0 when the node count is decremented to zero. At that time the microprocessor returns from the BSORT subroutine.

The bubble sort method can also sort signed or floating point numbers, or alphanumeric strings. To sort 16-bit signed numbers, for example, assume that the sign of the number is stored in the most significant bit of the 16-bit number. If the sign bit is a logic 0, the number is positive, and if the bit is a logic 1, the number is negative. The bubble sort subroutine in Table 3 performs the same operations as that in Table 2, except that the difference between the starting and final addresses of the list has to be divided by two, since each 16-bit number (node) requires two 8-bit memory locations for storage. Also, the microprocessor cannot execute any 16-bit comparison instructions, so two 8-bit subtractions must be performed.

One difference between the two subroutines is that the microprocessor has to check the signs of the two nodes being compared. If the sign of both numbers is the same (both positive or negative), the 16-bit comparison can be performed as usual. However, if the sign of the two numbers is different, the microprocessor

must ensure that the positive number is stored in the higher memory locations.

In Table 3, the microprocessor first subtracts the starting address in register pair H from the final address in register pair D. Note that the final address is the one in which the least significant byte (LSBY) of the last number is stored. After the 16-bit final address is subtracted, the 16-bit result is rotated once to the right, since each node requires two memory locations for storage. The most significant byte (MSBY) of the result must be rotated to the right first, followed by the LSBY.

At PASS1, the starting address of the list and the node count are saved on the stack. Register C is set to 0 to indicate that no exchanges have taken place. Starting at UP1, the node count in register pair D is again saved on the stack. The first 16-bit node is then moved to register pair D. The LSBY of the node is moved to register E and the MSBY (including the sign bit) is moved to register D. The address in register pair H is incremented twice, so that it addresses the memory location containing the MSBY and sign bit of the second node. The MSBYs of both nodes are then exclusive-ORed, and if the signs of the numbers are different, the microprocessor jumps to POSNEG, and must determine which number is positive and which is negative. Therefore, the microprocessor gets the MSBY from the node in memory, and performs an OR operation with itself to set the microprocessor's flags. If the number in memory is negative, the microprocessor jumps to EXCH, so that the negative number is moved to a lower memory address and the positive number is moved to a higher memory address. If the number in memory is positive, the two numbers are in the proper order, so the microprocessor simply jumps to OKASIS, when the node count is decremented and the exchange indicator is examined.

If the numbers are both positive or both negative, the microprocessor does not execute the JM to POSNEG stored in memory just before SUB2. Instead, the 16-bit number in memory is subtracted from the 16-bit number in register pair D. If the content of memory is greater than or equal to the content of register pair D, the microprocessor jumps to DWN1, because the numbers are in the proper order. If the content of memory is less than the content of register pair D, the microprocessor executes the instructions at EXCH.

The instructions at EXCH move the node addressed by register pair H to register pair B. The larger of the two is then moved from register pair D to memory. The memory address in register pair H is decremented so that the smaller node in register pair B can be saved in memory, at a lower memory address. The two nodes have now been exchanged, so the exchange indicator (register C) is set to 377.

Regardless of whether or not an exchange has taken place, the microprocessor executes the instructions at OKASIS when two nodes have been compared (and exchanged, if required). The instructions at OKASIS cause the node count to be popped off of the stack. The node count is decremented and examined to see if it is equal to zero. If it is not (indicating that additional nodes in the list must be examined), the microprocessor jumps back to UP1, where the decremented node count is saved on the stack and the compare and exchange instructions are executed again.

If the node count is decremented to zero, the JNZ to UP1 is not executed. The microprocessor has completed a pass through the list, so it must check the state of the exchange indicator. To do this, it pops the original node count and the starting address of the list off of the stack. The exchange indicator is then moved to register A, where an OR operation is performed with

TABLE 2

List-Sort Subroutine Using Exchange Method (Bubble Sort)

```
/THIS SUBROUTINE USES BUBBLE SORT ALGORITHM
/TO SORT SINGLE-PRECISION (8-BIT), UNSIGNED
/NUMBERS STORED IN MEMORY. ENTER THIS
/SUBROUTINE WITH STARTING ADDRESS OF LIST
/(LOWER ADDRESS) IN REGISTER PAIR H AND
/FINAL ADDRESS IN REGISTER PAIR D.
BSORT,  MOVAE   /GET LO BYTE OF HIGHEST
                /ADDRESS
        SUBL    /SUBTRACT BEGINNING LO
                /ADDRESS
        MOVEA   /SAVE RESULT IN E
        MOVAD   /GET HI BYTE OF HIGHEST
                /ADDRESS
        SBBH    /SUBTRACT BEGINNING HI
                /ADDRESS
        MOVDA   /SAVE RESULT IN D
PASSI,  PUSHH   /SAVE INITIAL ADDRESS
        PUSHD   /SAVE BYTE COUNT ON STACK
        MVIC    /REGISTER C IS USED TO INDICATE
        000     /IF AN EXCHANGE TAKES PLACE
UPI,    MOVAM   /GET A NODE FROM LIST
        INXH    /INCREMENT H AND L TO NEXT NODE
        CMPM    /COMPARE A AND MEMORY
        JC      /IF MEMORY >A, DO NOT
                /EXCHANGE THEM
        NEXT    /INSTEAD, EXAMINE NEXT
        0       /TWO NODES IN LIST
        JZ      /IF THEY ARE EQUAL, DO NOT
        NEXT    /EXCHANGE THEM EITHER
        0
        MOVBM   /SAVE CONTENT OF MEMORY IN B
        MOVMA   /SAVE CONTENT OF A IN MEMORY
        DCXH    /BACK UP 1 MEMORY LOCATION
        MOVMB   /AND THEN SAVE CONTENT OF
                /B IN MEMORY
        INXH    /INCREMENT LIST ADDRESS
        MVIC    /REGISTER C IS USED TO INDICATE
        377     /THAT AN EXCHANGE HAS TAKEN
                /PLACE
NEXT,   DCXD    /DECREMENT COUNT
        MOVAD   /IS COUNT 000?
        ORAE
        JNZ     /HAVE NOT CHECKED ENTIRE
        UP 1    /LIST, SO KEEP CHECKING
        0
        MOVAC   /GET EXCHANGE INDICATOR INTO
        ORAA    /REGISTER A AND SET FLAGS
        POPD    /LOAD D AND E WITH BYTE COUNT
        POPH    /LOAD H AND L WITH INITIAL
                /ADDRESS
        JNZ     /EXCHANGE OCCURRED, SO
        PASS 1  /EXAMINE LIST ONE MORE TIME
        0
        RET     /RETURN WHEN NO EXCHANGES
                /TAKE PLACE
```

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TABLE 3

Bubble Sort Subroutine for 16-Bit Signed Numbers

```
          *050 000
BSS16,    MOVAE     /GET FINAL ADDRESS (LSBY)
          SUBL      /SUBTRACT INITIAL ADDDRESS
                    /(LSBY)
          MOVEA     /SAVE RESULT (LSBY)
          MOVAD     /GET FINAL ADDRESS (MSBY)
          SBBH      /SUBTRACT INITIAL ADDRESS
                    /(MSBY)
          RRC       /DIVIDE RESULT BY TWO
          MOVDA     /AND SAVE IT
          MOVAE     /THEN DIVIDE LSBY OF
          RRC       /RESULT BY TWO
          MOVEA
PASS1,    PUSHH     /SAVE STARTING ADDRESS OF
                    /LIST
          PUSHD     /SAVE NODE COUNT
          MVIC      /SET EXCHANGE INDICATOR TO
          000       /ZERO
UP1,      PUSHD     /SAVE NODE COUNT
          MOVEM     /GET LSBY OF A NODE
          INXH      /INCREMENT MEMORY ADDRESS
          MOVDM     /GET MSBY OF SAME NODE
          INXH      /INCREMENT ADDRESS TWICE
          INXH      /TO MSBY OF NEXT NODE
          MOVAM     /GET ITS MSBY INTO A REGISTER
          XRAD      /EX OR IT WITH MSBY IN D
          JM        /IF ONE OF THE NUMBERS IS
          POSNEG    /NEGATIVE, FIND OUT WHICH
                    /ONE
          0
          DCXH      /DECREMENT ADDRESS TO LSBY
SUB2,     MOVAE     /BOTH NUMBERS ARE POSITIVE
          SUBM      /OR NEGATIVE, SO "COMPARE"
                    /THEM
          MOVBA
          INXH
          MOVAD     /NOW GET ONE OF THE MSBYS
          SBBM      /SUBTRACT THE OTHER
          JC        /CONTENT OF MEMORY IS
          DWN 1     /LARGER THAN CONTENT OF
                    /REGISTER PAIR D,
          0         /SO ORDER IS CORRECT
          ORAB      /NO CARRY, ARE THEY EQUAL?
          JZ        /YES, THEN DO NOT EXCHANGE
                    /THEM
          DWN 1
          0

EXCH,     MOVBM     /GET MSBY OF SECOND NUMBER
          MOVMD     /SAVE MSBY OF FIRST NO
          DCXH      /DECREMENT TO LSBY
          MOVCM     /GET LSBY OF SECOND NO
          MOVME     /SAVE LSBY OF FIRST NO
          DCXH      /DECREMENT TO MSBY
          MOVMB     /SAVE MSBY OF SECOND NO
          DCXH      /DECREMENT TO LSBY
          MOVMC     /SAVE LSBY OF SECOND NO
          INXH      /INCREMENT TO MSBY
          INXH      /THEN TO LSBY
          MVIC      /THEN SET EXCHANGE
          377       /INDICATOR TO 377

OKASIS,   POPD      /POP NODE COUNT
          DCXD      /DECREMENT IT
          MOVAD     /GET MSBY OF NODE COUNT
          ORAE      /OR IT WITH LSBY
          JNZ       /IS COUNT ZERO? NO, THEN
          UP 1      /EXAMINE NEXT TWO NODES
          0
          POPD      /YES, POP SECOND NODE COUNT
          POPH      /AND STARTING ADDRESS OF
          MOVAC     /LIST. WHAT IS STATE OF
          ORAA      /EXCHANGE INDICATOR?
          JNZ       /AN EXCHANGE TOOK PLACE, SO
          PASS 1    /EXAMINE LIST AGAIN
          0
          RET       /NO EXCHANGES TOOK PLACE,
                    /RETURN

POSNEG,   MOVAM     /IS NEGATIVE NUMBER IN
                    /MEMORY?
          ORAA
          JM        /YES, THEN IT IS LESS THAN
          EXCH      /POSITIVE NUMBER IN REGISTER
          0         /PAIR D?

DWN1,     DCXH      /DECREMENT TO LSBY
          JMP       /AND THEN EXAMINE NEXT TWO
          OKASIS    /NODES IN LIST
          0
```

itself. If an exchange took place during the last pass through the list, the microprocessor jumps back to PASS1. If this happens, register pair D contains the node count and register pair H contains the starting address of the list. If no exchanges took place during the last pass through the list, the content of register C is 0, so the microprocessor returns from the BSS16 subroutine. The 16-bit signed numbers contained in the list have now been sorted.

Reasons for sorting lists may simply be the fact that a program may execute faster if it has to access these lists or that alphanumeric strings may have to be sorted before being printed. While many sorting methods are much faster than the bubble sort, very few of them are easier to write.

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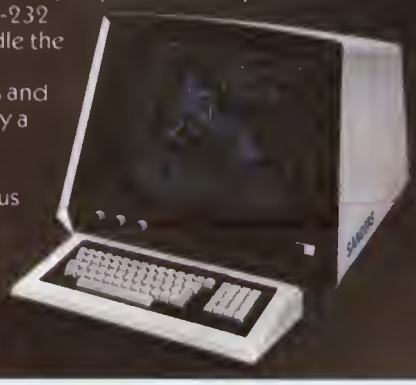

CIRCLE 70 ON INQUIRY CARD

Microcomputer Capabilities Are Stressed By Operating System and Software Tools

To provide for high performance microcomputer operations and maintain product compatibility at the same time, Data General Corp, Rt 9, Westboro, MA 01581, has developed an advanced operating system with utilities, a macro assembler, and support of two high level languages—specifically for 16-bit microcomputers. For development operations, the MICRON operating system runs on the original microNOVA and the recently announced MP/100 and /200 microcomputer systems (see *Computer Design*, May 79, pp 238, 243) with a disc or diskette subsystem. In runtime environments, it operates on any microprocessor based on microNOVA chip technology. It may be configured with or without the disc for dedicated applications.

The multitasking, realtime operating system provides for lower maintenance costs and increased programming productivity with such system development facilities and utilities as the interactive debugger and high level MP/PASCAL and MP/FORTRAN IV languages. The operating system is suited to instrumentation, industrial control/automation, education, scientific, and commercial applications.

Providing efficient data and memory management, the system has a modular internal structure and performs consistency checks on code and data to maximize reliability. A user selects only the routines needed for the operation. The system maintains disc file integrity through its fixup utility which automatically validates the disc structure at initial system load.

The advanced file management structure provides multiple levels of directories. Random access files address any record or disc with a single seek for maximum data throughput. Data management capabilities include permanent file protection, device independent I/O access, and hierarchical file directories to catalog programs and data.

Compatibility exists between MICRON and the company's Advanced Operating System (AOS) used on scientific and commercial ECLIPSE systems. Thus, users can create application programs that run on a small microNOVA chip or board microcomputer, as well as on a large ECLIPSE system.

Most of the utilities are operationally compatible with AOS. The command line interpreter (CLI) utility is a subset of the AOS CLI; it features a free format, English language style for writing full word commands or for using abbreviations. The CLI macro capability combines several related routines under one command.

Dedicated application programs developed under the operating system can also be burned into P/ROM. Creation of nonvolatile programs in main memory for applications not requiring magnetic peripherals reduces system overhead.

Users create, modify, and merge text files with the text editor. The binder utility combines object files and libraries to form program and overlay files.

Typical system requirement is any microNOVA with 64k bytes of memory and 1M bytes of disc or diskette storage. The runtime environment requires any microcomputer with 8k bytes of P/ROM and/or RAM. An AOS/MICRON development system requires an ECLIPSE computer licensed to run AOS with a disc and at least 256k bytes of memory.

Suited to programming, scientific, and business uses, MP/PASCAL is a structured programming language that features simple syntax and logically organized data structures. This logical approach results in faster development and more reliable code. Wirth's PASCAL is the foundation of this language, with Data General extensions added for the production programming environment.

The extensions include dynamic string data types, separate compilation modules, file I/O extensions, and an assembly language interface. With the string data types, strings are defined as dynamic structures whose length can vary from transaction to transaction. The compilation modules allow users to group routines and data that are common to many application programs.

Access is provided to all MICRON capabilities, including creation, deletion, and interactive random access of disc files. Also included is access to assembly language modules for critical code or control paths, and a direct system call function for high level access to all system capabilities.

A facility allows users to define data types or to use the character, integer, real, or Boolean primitive data types inherent in the language. In addition, data types may be referred to by pointers, which allow data reference passing, record linking, and dynamic allocation.

MP/FORTRAN IV is a variation of ANSI '66 FORTRAN with realtime extensions, thus allowing standard formatted and simplified I/O including free form programmed I/O, or conversational I/O through the keyboard. Data types include integer, real, double precision real, and complex variables, and built-in predefined mathematical functions. Useful in industrial, scientific, and statistical applications, the language also features multitasking "prommable" programs; flexible use of constants in parameter statements; and a subroutine library for accessing the operating system capabilities.

Additionally, the language allows variable names up to 31 characters long and arrays with up to 128 dimensions. It is compatible with DOS, RDOS, and AOS FORTRAN IV. Other characteristics are double precision and mixed mode arithmetic; relational and logical operators; user program swaps, chains, and overlays; and compiler generated reentrant coding.

Circle 410 on Inquiry Card

1M-Bit Bubble Memory Offers Nonvolatility for μComputer Applications

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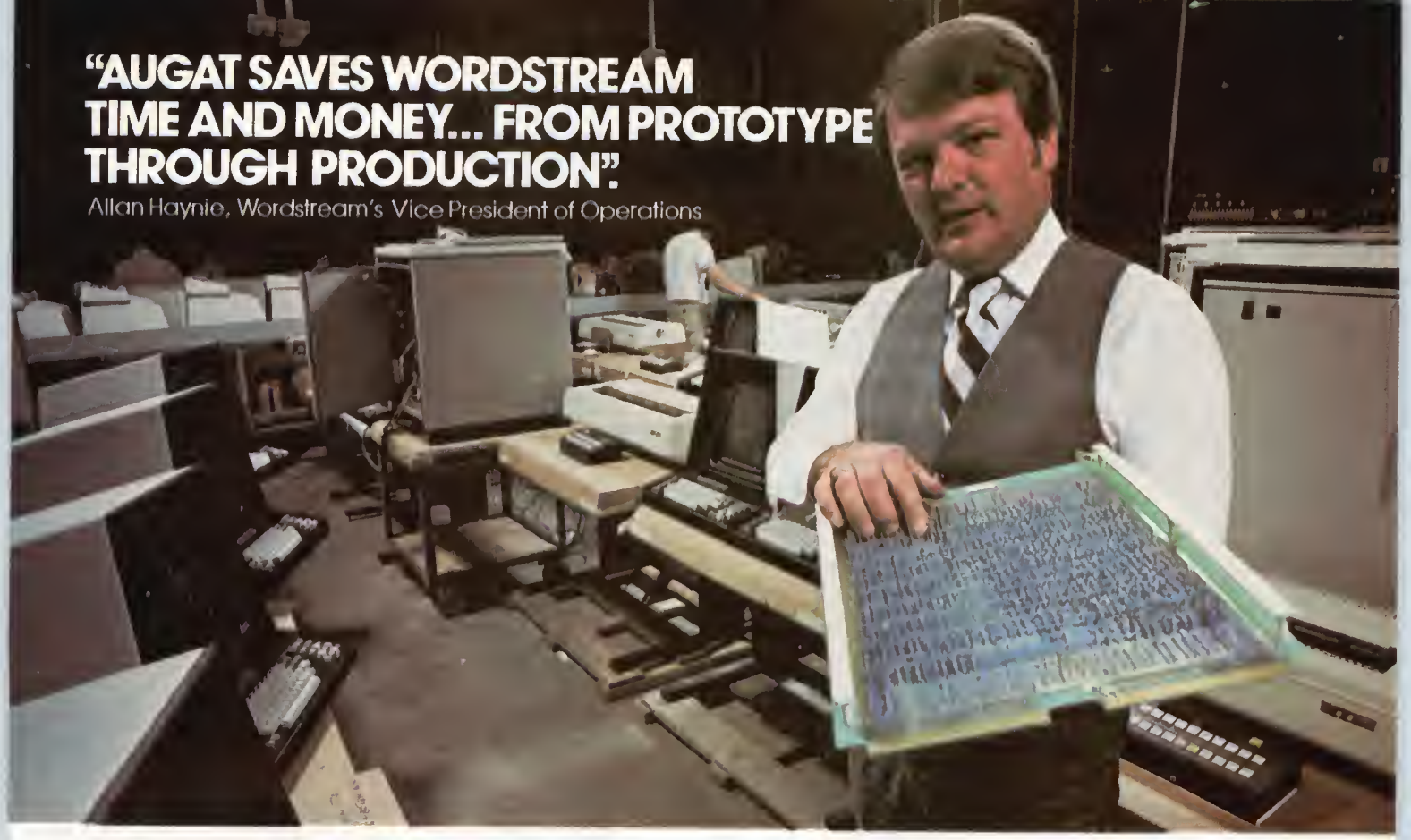
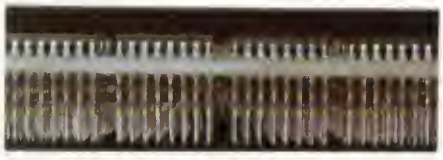


The Wordstream Corporations are subsidiaries of MAI Inc. They manufacture and market the Wordstream™ word processor, a shared logic system capable of handling 12 video display terminals, 10 diskette drives and three printers at once.

At the heart of the Wordstream system, you'll find Augat wirewrap* panels. Allan Haynie, Wordstream's Vice President of Operations, gives the details. "We use a large Augat board with about 250 integrated circuit chips in each printer station, diskette station, visual display and CPU. These boards are fabricated for us at Augat manufacturing facilities in Attleboro and Mashpee, Massachusetts and El Campo, Texas. Wire-wrapping is performed at their Datatex subsidiary in Houston."

At one time, Wordstream assembled their own IC panels. When asked why they switched to Augat wire-wrap, Allan Haynie replied, "basically, there were two reasons—the economy of Augat wirewrap panels and the service of Augat engineers. For example, Augat people worked closely with ours to develop a prototype board using their Data-logic™ computer-aided design service. They also designed the most economic way to wrap the boards. As a result, we've saved time and money during our prototype and design stages."

In the past, some users felt that wire-wrapping was not cost effective in large volume programs. Wordstream's experience shows that the opposite is true. Says Haynie, "because Augat supplies completely wired boards, our in-process inventory costs are significantly reduced. In addition, Augat panels give us the flexibility to implement design changes on the production line and in the field quickly and easily. We don't have to replace boards, just rewire them. And that means we can assure our customers that



their Wordstream system will always remain at the state of the art.

Even our final quality control is simplified with IC's replaced right at the test stations quickly and easily with no need for routing through production."

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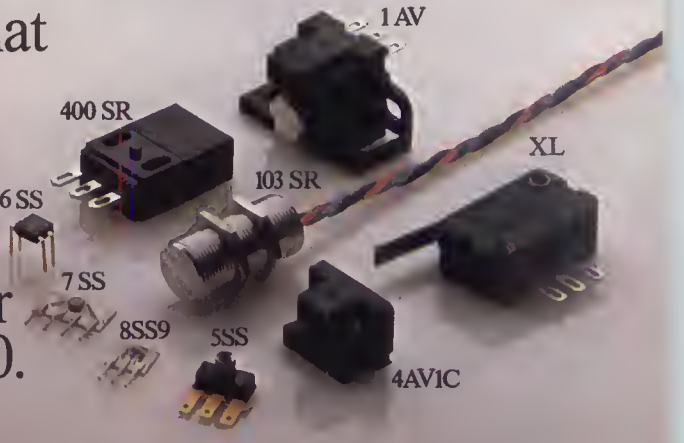

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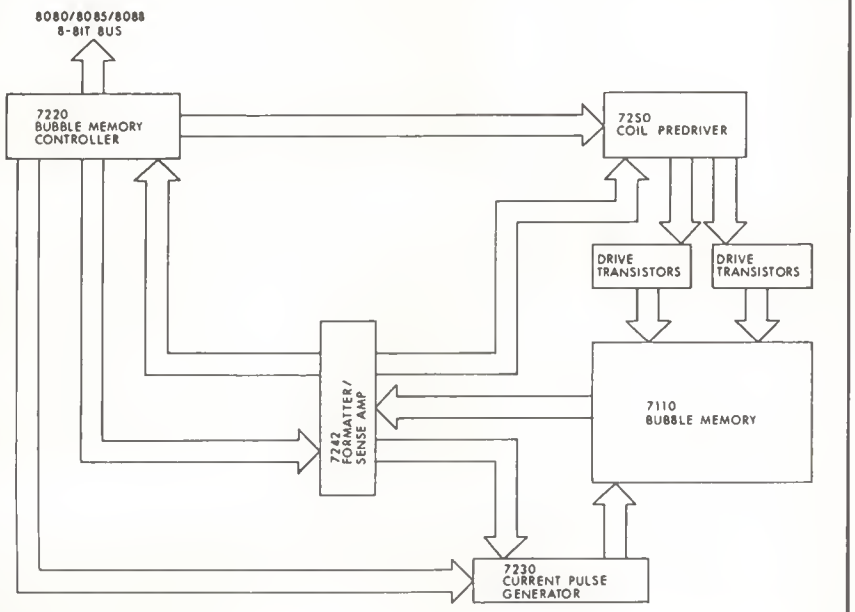
*Production quantity prices for the 8SS9 and 4AV1C, respectively.

CIRCLE 72 ON INQUIRY CARD



Support LSI circuits available with Intel Magnetics' 7110 magnetic bubble memory turn it into complete memory system featuring 1024k-bit storage density, high reliability, and nonvolatility

peripheral R/W memories are data terminals, word processing and other business systems, industrial control systems, and telecommunications systems.

The 7110 bubble memory uses block replicate architecture (see *Computer Design*, "Around the IC Loop," Apr 79, p 168); it is organized as a serial in—parallel loop storage—serial out shift register. In operation, a page or burst of pages up to the entire 2048 can be read or written at one system request. The device can be started and stopped between sequential pages for controlled rapid access. The average random access time is 40 ms, max data rate is 100 kHz, R/W time is 6.5 ms, and the average data rate is 78 kHz.

Additional storage is built-in, partly for error detection and correction of burst errors up to five bits in length, and partly for increasing production yield by allowing some loops to be defective. For the latter, the device includes 48 redundant loops and an internal code that makes unused loops transparent to the user.

Various configurations can increase system capacity. One 7220 controller can operate up to eight 7110 devices in parallel for increased speed, or eight multiplexed one, or two, or four at a time to conserve power. The system can transfer data to the system bus through polled I/O, interrupt driven I/O, or DMA.

The memory, developed by Intel Magnetics, 3000 Oakmead Village Dr, Santa Clara, CA 95051, exhibits high reliability of semiconductor devices; in addition, a chief advantage is nonvolatility. It is resistant to shock, vibration, humidity, and radiation, suiting it for harsh environments. The system operates from standard 12- and 5-V supplies.

User interface is provided by the 40-pin 7220 bubble memory controller. It provides bus interface, generates all memory system timing and control, maintains memory address information, and interprets and executes user requests for data transfers.

The 20-pin 7247 formatter/sense amplifier (FSA) is a dual-channel unit that interfaces both channels of the memory, and has burst error detection and correction circuits for each channel. It senses the low level bubble signals, handles redundant loops, and buffers data. The 22-pin 7230 current pulse generator (CPG) supplies the necessary relatively high peak currents. It also contains power failure detect and power-down circuits. High currents with peaks beyond the capacity of standard ICs are required to drive the coils; therefore, the 16-pin 7250 coil predriver (CPD) interfaces the 7220 BMC to driver transistors.

These support circuits serve as flexible control and interface between the system bus and bubble memory array. By replacing a board of control electronics, they make it practical for OEMs to use the memory in production products.

Price of the 7110 prototype kit to build a magnetic bubble memory system into new products is approximately $2000. Deliveries will begin this fall.

Circle 411 on Inquiry Card

Simple to Use, Low Power Units Customize µComputer Equipment

Providing ready to use hardware for custom applications of microcomputer equipment, Microboard Milliwatt computer systems are manufactured by RCA Solid State Div, PO Box 3200, Somerville, NJ 08876, using low power CMOS with static operation. These circuits are three computers, four memories, and five expansion modules, all on 4.5 x 7.5" (11.4 x 19-cm) PC boards, plus a power converter and three chassis. All units are expandable and interchangeable using the COSMAC Microboard universal backplane; they also are compatible with the COSMAC development systems.

CDP18S601, 602, and 603 are complete systems with a CDP1802 COSMAC microprocessor, crystal controlled clock, R/W memory, parallel

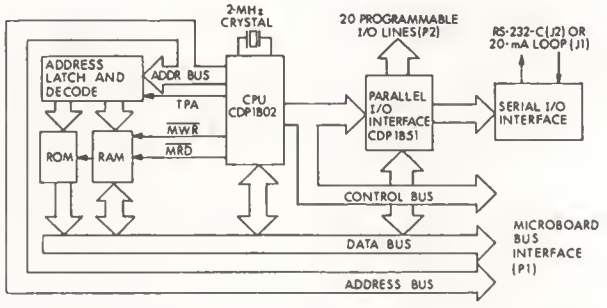
I/O ports, serial communication interface, power-on reset, an expansion interface, and sockets for ROM. The 601 and 603 utilize a CDP1851 CMOS programmable I/O interface to provide 25 I/O lines; the 602 uses a CDP1854 UART for 21 I/O lines. Provisions for either RS-232-C or 20-mA serial I/O, four flag inputs, and Q serial data output are included. Powered from a single 5-V supply, they require only 7 to 10 mA when operated without EPROM or 20-mA loop interface. The systems can have up to 8k bytes on board in a 64k-byte memory space.

The four memories are the CDP18S620, a 4k-byte RAM; the 621, a 16k-byte RAM; the 622, an 8k-byte RAM with battery backup; and the 625, an 8k/16k-byte ROM-P/ROM with eight sockets for CDP1834 ROMs or 2708, 2758, or 2716 EPROMs. Also included is a CDP18S641 UART interface featuring a CDP1854 UART in the programmed COSMAC mode, a 20-mA or an RS-232-C serial interface, selectable baud rate of 110 to 19.2k, paper tape-reader run control, and assignable I/O address.

Combination memory and I/O unit —CDP18S660—features 40 programmable I/O lines, 2k bytes of CMOS RAM, and four sockets for up to 8k bytes of EPROM or 4k bytes of mask programmable ROM. Other components are the CDP18S642 DAC; 643 ADC; 640 control and display module; 023 COSMAC power converter, a regulated 5-V, 600-mA supply; the 675 5-card chassis with preprinted Microboard universal backplane for all five cards; 25-card chassis with case and power supply; and the 480 P/ROM programmer.

A fully assembled Microboard Prototyping System (CDP18S691) is also offered to speed up and simplify microcomputer design. It consists of the 601 Microboard computer, the control/display module, 5-card chassis, 5-V power converter, Microboard breadboard, cables, connectors, and a 1k-byte ROM based utility system with editing commands. The system has a 6-digit hexadecimal display. Four control switches provide reset, run program, run utility, and step-continuous.

Circle 412 on Inquiry Card



Microboard computer systems (CDP18S601 and 603) from RCA plug onto Microboard 5- or 25-card chassis with COSMAC Microboard Universal backplane. Ready to use series of CMOS modules customize applications, permitting users to begin software development

µComputer Printers Feature Flexible Paper Handling System

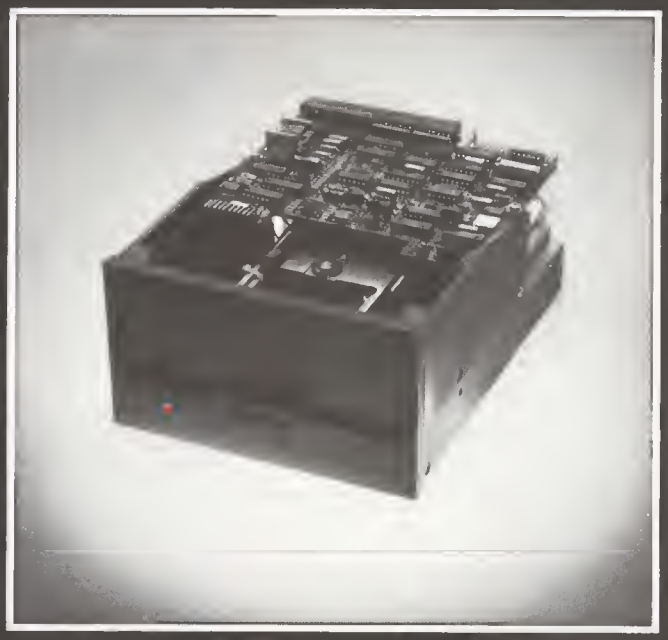
The 730 series of dot matrix printers are intended for the microcomputer market consisting of personal, very small business systems, and terminals. The family includes the model 730-1, a parallel interfaced 60-Hz unit, and model 730-3, a serial interfaced 60-Hz unit. Both have an upper/lower case 96-char U.S. ASCII set. Four European models are the 730-2, a parallel interfaced 50-Hz unit with 96-char U.S. ASCII set; the 730-4, a similar serial interfaced printer; and models 730-5 and -6, parallel and serial interfaced, respectively, with five switch selectable European character sets as well as the 96-char U.S. ASCII code. The parallel interfaced 730-7 includes a Katakana character set for Japanese markets, and operates at 50/60 Hz, 100 V.

Centronics Data Computer Corp, Hudson, NH 03051, uses the same heavy duty, free flight printhead technology found in the computer grade 700 series printers. This produces a 7 x 7 dot matrix. Other features, chosen to keep the price as low as $995, are 80-col line lengths at 10 char/in (4/cm), an 80-char buffer, 50 char/s, unidirectional print at 5 in (13 cm)/s, high speed return of approximately 10 in (25 cm)/s, and 6 lines/in (2.4/cm) vertical. Electronics are based on an 8049 microprocessor. A continuous mobius loop ribbon allows printing on upper and lower portions on alternate passes.

The compact unit weighs less than 10 lb (5 kg) and measures 14.5" (37 cm) wide by 11.0" (28 cm) deep by 4.89" (13 cm) high. Mechanical moving parts are minimized to ensure reliability and serviceability.

A three-in-one paper handling system is a key feature. The printer handles roll paper, fanfold, and cut sheets. The typewriter like platen accepts up to three hand-fed sheets with two carbons—8.5" (21.6 cm) wide in letter, legal size, or longer lengths, as well as international sized A4 sheets. Fixed pins on the platen accept standard computer grade multipart or single-part fanfold paper that is 9" (23 cm) wide from pin to pin. Finally, the system can use 8.5" (21.6-cm) wide roll paper up to 5" (13 cm) in dia, with the attachment of a standard paper holding rack. A built-in tear bar permits paper tear off within five lines of print.

Circle 413 on Inquiry Card



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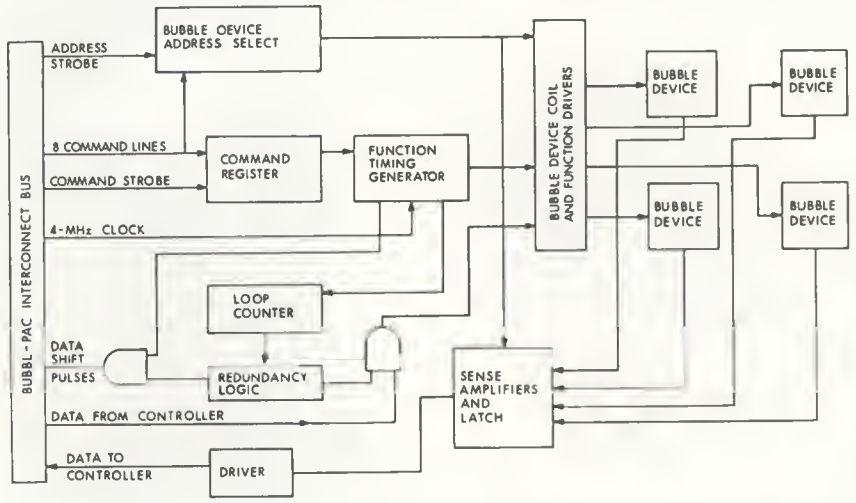
CIRCLE 73 ON INQUIRY CARD

Module Controls Up to 16 Bubble Memory Units For Nonvolatile Storage



Bubbl-Tec's memory system consists of controller and Bubbl-Pac bubble memory module (diagrammed) that is replicated up to 16 times. System performs write, seek, and read operations; it is easily incorporated into any LSI-11 microcomputer requiring reliable, nonvolatile memory without moving mechanical parts

BUBBL-MACHINE™ magnetic bubble add-in memory installs directly into Digital Equipment Corp's LSI-11 microcomputer card cage. The system consists of one dual-height MBC-11 BUBBL-BOARD™ controller module and from one to 16 dual-height BUBBL-PAC™ bubble memory modules, each containing 40k bytes of nonvolatile data. Modules connect to the controller in daisy chain fashion via 26-conductor ribbon cables.

Based on a Z80 microprocessor, the controller is command compatible with DEC RXV11/RX01 floppy disc protocol. The microprocessor handles bubble device formatting and control, as well as interfacing the bubble memory system to the LSI-11 bus structure. The controller maps standard floppy disc track and sector addresses into bubble device page addresses, so that the memory is compatible with all DEC software for the LSI-11.

The ready-to-operate system has no moving parts and offers nonvolatile storage. Media are Texas Instruments' TIB0203 92k-bit magnetic bubble memory devices. Each device is organized as 157 minor loops, similar to shift registers. During manufacture, certain of these loops are often found to be defective and cannot be used. To prevent writing into or reading from these loops, an inhibit bit is stored in a redundancy ROM address that corresponds to the position of the bad loop. This bit prevents data from being written into bad loops, and inhibits the data shift pulses to the shift register.

Six memory modules in the system from Bubbl-Tec div, PC/M Inc, 3120 Crow Canyon Rd, San Ramon, CA 94583, gives storage equal to that of a single-density floppy disc. Access time to the first data byte averages less than 7 ms; seek time is 6.4 ms max. Power consumption is less than 20 W. The controller is priced at $650 and the bubble memory module at $950, both in single quantities.

Circle 414 on Inquiry Card

Architecture of CMOS µComputer Version Suits EPROM Based Devices

The IM87C48 single-chip CMOS EPROM based 8-bit microcomputer is a pin for pin and function for function edition of Intel's NMOS 8748 microcomputer. It offers inherent CMOS advantages of low power requirements, high noise immunity, and operation at extended temperature ranges, and its architecture is appropriate for EPROM based devices. Low power dissipation is less than 50 mW at 5 V; operating temp range is −40 to 85 °C.

Components are a CPU, 1k bytes of EPROM, 64 bytes of RAM, 27 I/O lines, and an onchip counter/timer for realtime applications. The I/O lines serve as static bidirectional ports or interfaces to external memory and I/O expander circuits. CPU instructions can test three of the input lines to perform conditional jumps. External memory devices added to the microcomputer result in systems of up to 4096 bytes of program memory and 256 bytes of data memory.

The set of over 90 instructions has bit set/reset functions as well as those that control an onchip counter/timer. An 8-level subroutine stack and 16 general purpose registers ease data flow, provide direct and indirect addressing modes, and implement subroutine calls.

Additional devices that will share the architecture and instruction set are the IM82C43 I/O expander, an IM80C49 2k x 8 ROM/128-byte RAM microcomputer, an IM80C48 1k x 8 ROM/64-byte RAM device, an IM80C41 1k x 8 ROM/64-byte RAM port, and an IM80C35 external ROM/EPROM, 64-byte RAM microcomputer. All of these are announced or available in NMOS from Intel, NEC, National, and Signetics.

Intersil, Inc, 10710 N Tantau Ave, Cupertino, CA 95014, is also sampling the IM87C41, a programmable peripheral interface microcomputer (PPIM) with 1k x 8 EPROM/64-byte RAM architecture. The IM80C42 2k x 8/128-byte RAM PPIM, which has no current NMOS equivalent, will soon be added to the family.

The microcomputer's configuration assists the user in debugging soft-

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SILONICS
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ware and hardware prototypes. A single-step pin allows stepping through the program, and the EPROM permits software to be put through trial runs before it is committed to ROM. It can also operate with substituted external memories, allowing construction of simple prototyping aids using RAM in place of EPROM for easy program changes. The IM87C48 in a 40-pin CERDIP is priced at $82.50 in single-unit quantities.

Circle 415 on Inquiry Card

µProcessor Industrial Control Systems Are Custom Configurable

Offboard interface modules, consulting and custom design capabilities, and use of field programmable logic arrays (FPLAs) to implement a library of 6800 based software are capabilities of the SYS-68 family of microprocessor cards that suit them to OEM industrial control and instrumentation uses. Systems range from a single-board computer (SBC) to a fully software supported disc development system that addresses up to 0.5M bytes of memory.

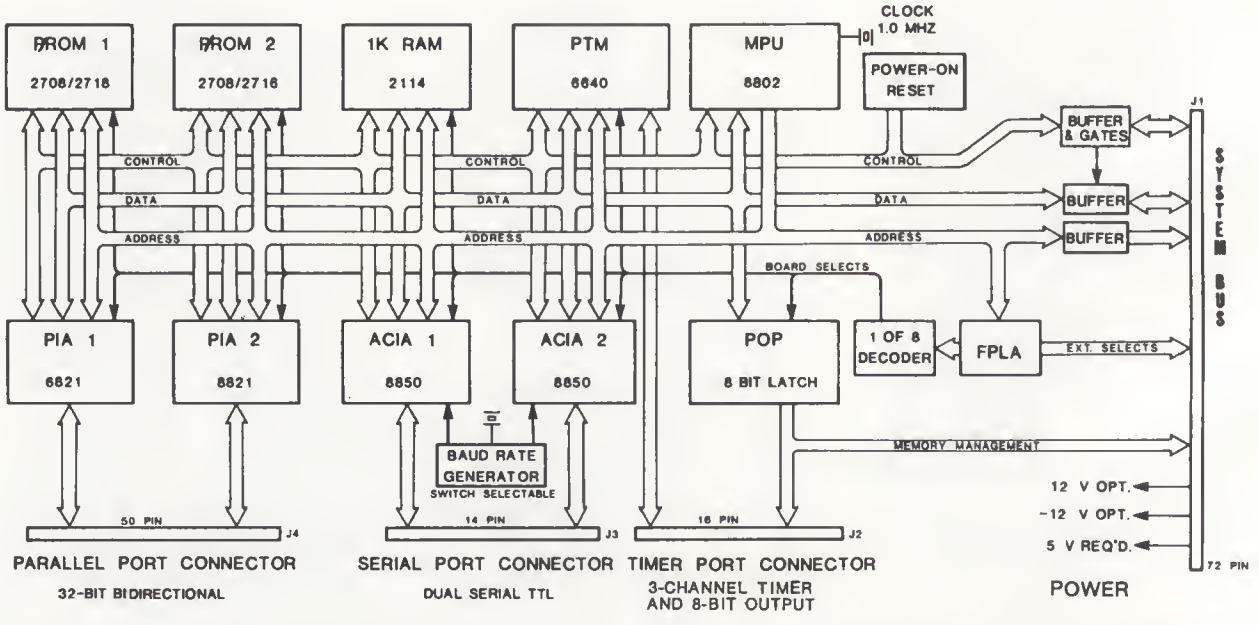
The MPU card (SBC) contains 1k of static RAM and up to 4k of P/ROM, features power-on reset circuitry, and is available in a single-supply (5-V) option. Onboard interfacing includes four 8-bit parallel I/O ports; two serial I/O ports; three channels of a 16-bit circuit for software controlled time, count, pulse, and interrupt functions; and an 8-bit latched output. An optional bidirectional interface driver module drives signals needing long cables or high currents.

Synetic Designs Co, 252 San Lorenzo, Pomona, CA 91766, supplements the family with offboard interface modules that allow manufacturers to purchase only the required hardware. The interface module mounting panel permits interchangeable I/O configurations and simple custom interface designs. These modules provide for dual opto-isolated TTY, dual EIA RS-232-C, 300-baud modem/RS-232-C, or fiber optic interface.

The SYS-68 MEM card supports up to 16k of static RAM and 8k or 16k of P/ROM (not supplied). Several utility boards which connect to the system via a ribbon cable provide for signal conditioning and power driving applications.

System cards measure 4.5 x 9.6" (11.4 x 24.4 cm), while the interface modules measure 4.5 x 2.5" (11.4 x 6.4 cm) with 1.0" (2.5-cm) wide panels. Inclusion of the FPLA reduces board decoding costs. A 72-instruction set is included in the processor.

Circle 416 on Inquiry Card



Sys-68 single-board computer from Synetic Designs is a 6800 based system that is configurable with additional memory, offboard modules, and software library to serve OEM industrial control and instrumentation applications. System cards require only 5-V power; P/ROM chips (2708) and interface modules (RS-232-C) require ±12-V supplies

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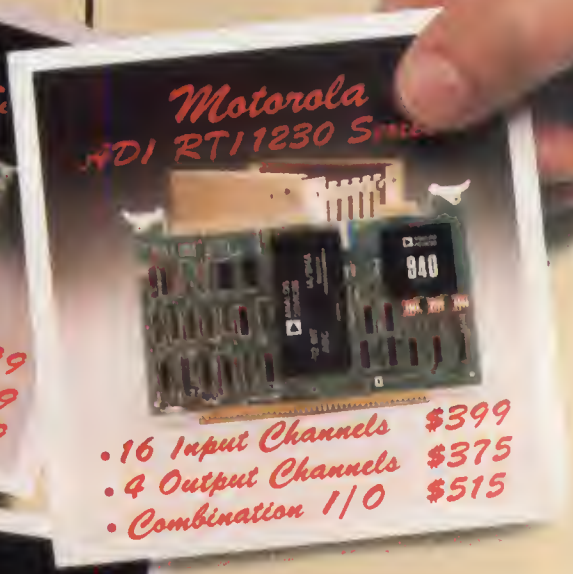

For complete information on the Analog Devices RTI Series Analog I/O Cards, write or call Analog Devices, P.O. Box 280, Norwood, MA 02062. Telephone: (617) 329-4700.

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For more information on: Intel 75, Motorola 76, Texas Instruments 77, Dec 78, Mostek 79, Pro-Log 80.

Microcomputer System Packs 8″ Winchester Rigid Disc Drive

The C8000 Z80 based microcomputer places a 10M-byte 8″ (20-cm) Winchester type rigid disc drive and a 12M-byte cartridge tape drive in a tabletop package. The disc has a 50-ms average access time and is completely backed up with a single cartridge on the tape drive in 20 min. Onyx Systems, Inc, 10375 Bandley Dr, Cupertino, CA 95014, has designed it for applications that require greater storage and performance than a floppy disc can provide. Peripherals including a system console, serial and parallel printers, and most standard modems are supported simultaneously.

Features are 64k bytes of dynamic RAM with parity (using 16k devices), a general purpose DMA controller, three general purpose RS-232 serial I/O ports, an 8-bit bidirectional parallel port with parity, and a realtime clock. A Z8000 upgrade package, available fourth quarter of 1979, will convert the Z80 board to an intelligent file system. This enables system support of up to 10 user terminals and networking of systems over a high speed local serial link.

Circle 417 on Inquiry Card

Onyx C8000 microcomputer system is pictured from above with cover removed. 10M-byte rigid disc drive (right) and 12M-byte cartridge tape drive (left) are revealed. Not shown is 4-MHz Z80A CPU board which mounts on hinged platform and covers drives and power supply

Microcomputers Serve Many Segments of Low End Market

Companion single-chip, 8-bit microcomputers are based on the Am8048, which has 64 bytes of RAM, 1k bytes of ROM, 27 I/O lines, an 8-bit interval timer/event counter, onboard oscillator, clock circuits, and a 2.5-μs instruction cycle CPU. Their use as realtime controllers requires efficient instruction sets; this is provided by bit-handling capabilities for both binary and BCD arithmetic. Of the over 90 instructions, 70% require a single byte; none takes more than two bytes.

The Am8041 variation is a slaveable microprocessor for use with Am9080A/8080A and Am8085 systems; one port becomes dedicated to the host data bus, and program and data memory are not expandable beyond 1k and 64 bytes, respectively. Other functional differences are the change of the external interrupt to a chip select, program-storage enable to port select, and read and write lines to input only.

Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086, processes all three devices to MIL-STD-883C requirements. For more capability, the Am8048 and Am8035 (an Am8048 without program memory) can be expanded using standard memories and Am9080A/8080A peripherals.

Circle 418 on Inquiry Card

Expansion Motherboard Alters Microcomputer By Adding External Memory

Key to using external memory with the AIM 65 microcomputer is a buffered expansion motherboard which Rockwell International, Electronic Devices Div, 3310 Miraloma Ave, PO Box 3669, Anaheim, CA 92803, is offering as an option for $195. The AIM 65 expansion motherboard has five connector slots that accommodate the company's SYSTEM 65 or Motorola EXORciser modules, as well as add-on modules from Burr-Brown and others.

Essentially, the motherboard extends the microcomputer bus (see *Computer Design*, Dec 78, p 136). Address, data, and control bus lines are buffered to provide ample drive capability. Address decode logic is provided for mapping internal and external addresses in 4k-byte increments. The user can define with 16 switches whether each 4k-byte portion of the R6502 CPU 65k-byte address space is internal or external to the microcomputer.

The expansion board adapts the microcomputer to a variety of applications. While originally designed as an educational aid, the microcomputer now operates with the company's 1M-bit bubble memory module, a tape recorder, or a modem for such uses as a distributed processing terminal, a development system, a smart terminal, and a process controller.

Circle 419 on Inquiry Card

Communications Modem Transmits Information Between Microcomputers

Micromodem II™ is a data communications system that transfers data between an Apple II microcomputer and another Apple II, another microcomputer, terminal, minicomputer, or timesharing computer. The modem converts digital data to analog signals for transmission over regular voice telephone lines.

Developed by D. C. Hayes Associates, Inc, 16 Perimeter Park Dr, PO Box 9884, Atlanta, GA 30319, the system includes serial I/O, 1k bytes of firmware, a 103 compatible modem, and FCC registered interface. The FCC registered Microcoupler™ data access arrangement feeds the signal into the telephone line through a modular connector provided by the local telephone company. Operation is at 110 or 300 baud (equivalent to 10 or 30 char/s).

Automatic dialing, automatic answering, and built-in programmed memory are provided in the package. All necessary programs are contained in ROM for operation in any of three modes—terminal mode, where the Apple II is used as a terminal; remote console, which allows another terminal to call the microcomputer; or program control, where BASIC programs are completed.

Circle 420 on Inquiry Card

Printer Produces TRS-80 μComputer Hard Copy On Aluminum Coated Paper

The TRS-80 Quick Printer II prints both upper and lower case characters as well as double-size and double-spaced characters. Automatic wrap-around prevents data loss due to overflow when the text exceeds the maximum line length.

The printer produces 120 lines/min, 64 char/s. The char set consists of a modified subset of ASCII, 96 char with upper and lower case, 5 x 7 dot matrix, and 6-line/in (2/cm) vertical spacing. It produces all 32 ASCII control codes in addition to codes for the printed character. The printer is software selectable for 16 to 32 char/line.

Radio Shack, a division of Tandy Corp, 1300 One Tandy Ctr, Fort Worth, TX 76102, claims that the printer, designed for Level II TRS-80 systems, can be used with various other computers as well; three standard interfaces are the TRS-80, RS-232-C, and 8-bit parallel. It connects directly to the TRS-80 CPU, or with an optional cable to the microcomputer expansion interface.

Circle 431 on Inquiry Card

Communication Interface Adds Controller Capability to μComputer

A GPIB-488 to Radio Shack TRS-80 microcomputer interface adds GPIB-488 controller capability to the computer. In addition, it allows full communication from BASIC to GPIB-488 devices. Measuring 5.25 x 17 x 13" (13.34 x 43 x 33 cm), the device requires 115 Vac/50 W.

Scientific Engineering Laboratories, 11 Neil Dr, Old Bethpage, NY 11804, has incorporated various commands. These initialize a GPIB control program, and address a specified device either as a listener or a talker. Another outputs a series of bytes to the bus as bus commands, or a series of characters as data; the latter inputs a series of bytes from an addressed talker on the bus.

Circle 432 on Inquiry Card

Open Frame Power Supply Provides Closely Regulated dc Voltage

Microprocessor compatible output voltages are provided by the model 7248 supply, which incorporates a large metal chassis for easy mounting while simultaneously providing the required heat sinking. The power supply outputs 12 V at 1 A, −12 V at 200 mA, 5 V at 6 A, −5 V at 100 mA (±12 and 5 are adjustable ±5%). Specifications include line and load regulation of 0.1%, ripple of 2 mV rms, tempco of 0.02%/°C, and temp range of 0 to 50 °C.

Calex Mfg Co, Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523, has also included continuance foldback current limiting, overvoltage protection, and input of 115/230 Vac ±10%, 47 to 440 Hz. The 8.0 x 4.5 x 4.0" (20.3 x 11.4 x 10.2-cm) units are all burned in.

Circle 433 on Inquiry Card

Raster Scan Monitor Generates High Resolution Graphics Display

Interfacing to DEC LSI-11, Zilog Z80, and Intel 8086 processors, GMDM-1000 uses a 15" (38-cm) monitor to generate a 1024 x 768-element display for graphics, document facsimile, or high density text application. Stability and clearness of display is produced by noninterlaced refreshing of the screen 60 times/s, coupled with low persistence phosphors on the monitor.

The unit displays the contents of a 0.75M-bit memory module. The program controlled host I/O functions allow individual memory words to be written and read. Three Boolean functions and bit mode are supported so that individually addressable bits can be accessed. The single PC board from Image Automation, Inc, 3350 Scott Blvd, Bldg 22, Santa Clara, CA 95051, can be packaged with an integral power supply in a 19" (48-cm) rackmountable enclosure.

Circle 434 on Inquiry Card

Data Acquisition System Accepts Boards to Adapt to Applications

System 2000 series data acquisition systems for industrial and scientific applications can contain, in a half-rack enclosure, a wide range of analog and digital I/O modules that plug into a bus structure identical to that used by Digital Equipment Corp in the LSI-11/2 and 11/23. Components of the system are the model 2000E half-rack closure, model 2000BP backplane with 13 bus slots and card cage, and 2000PS power supply. The unit's front panel is removable; the rear panel mounted fan cools the card cage and power supply, which supplies 5 V at 15 A and 12 V at 3 A.

Adac Corp, 70 Tower Office Pk, Woburn, MA 01801, has tailored the system—a companion unit to the System 1000—for half-quad (8.5 x 5", 21.6 x 13-cm) boards only, with positive retention of all plug-in modules. It can operate as a low cost peripheral expander to any UNIBUS computer by using the model 1900 UNIBUS to LSI-11/2 bus translator.

An integral 16-bit microcomputer can be included for overall control of the system operation in many applications. High speed communications are handled through a general purpose parallel interface module; a serialized output and input, conforming to RS-232-C specs, handle slower data transfer. A 20-mA current loop provides direct connection into the teletypewriter port of the host computer by running a twisted pair over distances up to 500 ft (152 m).

Analog inputs from low level (10 mV FS), high common mode voltage (250 V) to high level, high speed can be accepted. Modules can be supplied with software programmable gain amplifiers, high speed S/H amplifiers, and high speed ADCs.

Analog outputs are available in voltage or current loop format. Digital I/O modules can communicate with standard TTL or contact closure sources and standard TTL, or high current, high voltage loads, with isolation I/O also available.

Circle 435 on Inquiry Card

One way to order everything (all day on the phone)

Before he bought from Inmac, one customer required a pile of catalogs second only to Mt. Everest.

When the time came, he'd know just where to look for supplies.

A disk pack?
He'd go right to that 35-pound catalog under the philodendron.

A CRT stand?
Right to the furniture catalog. (Too bad he didn't read the fine print that said "2-month wait".)

EIA cables?
In the catalog that looked like last year's winning entry in the stump-the-engineer contest.

One day he needed a disk pack. And a CRT stand, 5 EIA cables, one box of thermal paper, 6 print-wheels and a harmonica ribbon.

If he didn't get them quick, he couldn't finish the Big Project. And top management was really breathing down his neck.

By the time he got all the catalogs together, figured out what would work with what, and made all the calls . . . 9 a.m. became 9 p.m.

And part of his order got stuck between Texas and Terre Haute.

Never again.

So he subscribed to the Inmac catalog. After all, 70 pages wasn't much for every supply he needed. Plus he could store it in a drawer.

He got rid of almost all those other catalogs. But his office looked empty. So he went out and bought a poster of Nepal.

With a great view of Mt. Everest.

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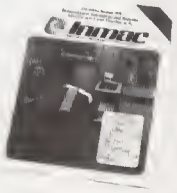
How you can get 1,000+ supplies and accessories. No hassle, no wait.

Order from the FREE Inmac catalog for precision performers. Magnetic media. Printer paper. Cables compatible with DEC, DGC, HP, TI and IBM hardware. Ribbons. Computer-room furniture. More. Guaranteed for 45 days. Some up to 10 full years.



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Inmac
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Corporate Address: 2465 Augustine Drive, Santa Clara, CA. 95051

CIRCLE 81 ON INQUIRY CARD

Microcomputer Power Supplies Meet Domestic and Foreign Standards

The 2000I series is an international version of the series of microprocessor power supplies being sold by Conver Corp, 10631 Bandley Dr, Cupertino, CA 95014. The 27-W output supply meets all domestic and foreign safety and rfi standards, including UL, CSA, VDE, and S.E.V. Customer changeable taps accommodate input voltages of 100/110/120/200/220/240 Vac, all 10 to 13%, 47 to 63 Hz.

The basic model, measuring 7.75 x 4.25 x 2.80" (19.69 x 10.80 x 7.11 cm), is rated at 5 V, 4 A, ±12 V, 0.3 A; a variable negative voltage is 0.2 A. Typ efficiency is 60%. Overload and overvoltage protection are included.

Circle 424 on Inquiry Card

Microcomputer Accepts Up to Four Single- or Two Double-Headed Drives

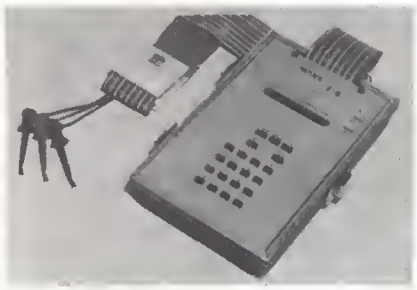
Single-head or dual-head add-on disc drives are offered by Microcomputer Technology, Inc, 2080 S Grand Ave, Santa Ana, CA 92705, for the Radio Shack TRS-80 computer. The single-head family (TF-X) offers MPI, Pertec, or Shugart SA400 minifloppy disc drives. Shugart drives are offered by Radio Shack; Pertec drives provide quieter operation and the Flippy diskette (uses both sides), while the MPI unit adds features such as door lock and automatic diskette ejection. The dual-headed units (TDH-X) provide the same capacity as two single-headed drives, while saving space. Prices start at $379 and $675, respectively. Interfacing is via the Radio Shack TRS-80 expansion interface; Radio Shack also offers operating software. Circle 425 on Inquiry Card

Design Engineering Tool Simplifies Microcomputer Debugging Job

Model T-8 analyzer, complementing microcomputer development systems, connects to the microcomputer under test via a 40-pin chip clip to single step the microprocessor or let it free run to a selected error vector or trap address. Internal trace capabilities examine 63 machine cycles which preceded the breakpoint. The 8½-digit display allows information to be displayed and the problem analyzed.

Patuck Inc, 5073 Russell Ave, Pennsauken, NJ 08109, is also aiming the tool toward designers developing microcode on a general purpose computer and field service technicians. Single-unit quantities are priced at $695. Optional microcomputer interfaces for the 8080, Z80, 2650, 6501, 6502, 6505, 8060, and 8085 cost $50 each.

Circle 426 on Inquiry Card



Compact Card Reader Offers Alternative to Keyboard Data Entry

The MR-500 mark sense card reader accepts cards of any length marked with a number two pencil. The user hand feeds the card into the unit which automatically turns on and converts data into either ASCII or card image. Chatsworth Data Corp, 20710 Lassen St, Chatsworth, CA 91311, is addressing educational and small business applications with special hardware and software interfaces that have been developed to connect the reader to TRS-80, Apple II, and PET computers. Other interfaces will also be added.

Circle 427 on Inquiry Card

MAKE YOUR NOVA PERFORM LIKE A FERRARI

...with the first Lifetime-Guaranteed Disc Controller

At Quentin Research, we don't call our revolutionary new Model N6010 Nova Compatible Disc Controller "The Cadillac of the Industry": it comes without "bells and whistles"... the luxury accessories you probably won't need and don't want to pay for.

Instead, Quentin's crack team of Advanced Technology Specialists has created a low cost, ultra-high speed controller that brings out the "Ferrari" in your basic Nova; permitting the computer to handle information at maximum disc speed: 9.67 MHz or 1.2 MBytes per second.

But in designing the N6010 as the fastest controller on the market, we haven't left off the important features: overlap seek, compatibility with RDOS, IRIS and BLIS/COBOL operating systems, and the capability to interface up to four CDC or other storage module disc drives with any Nova or Eclipse computer.

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CIRCLE 83 ON INQUIRY CARD

QUENTIN
Research, Inc.

What will they think of next?

SOFTWARE

Support Tools Reduce 6800 Program Development and Debugging Time

Six 6800 microcomputer programs—an assembler-linking loader, three disassemblers, a relocator, and a monitor with debugging capabilities—are available on cassette or disc (except the monitor which is in EPROM). Developed by Ed Smith's Software Works company, the programs work with operating systems offered by Percom Data Company, Inc, 211 N Kirby, Garland, TX 75042, for use in development and debugging.

Producing relocatable object code, the assembler and linking loader feature alphabetized cross reference listing, and global and local labels. Together they require less than 10k bytes of memory. Using this tool, the relocating disassembler and segmented source text generator package produces compacted code for reediting and assembly. A segmenting feature breaks down a large object program into small source modules; linkage references are automatically added. Both programs are furnished in relocatable formatted code.

The disassembler/source generator, requiring 4k bytes of RAM, produces compacted source code for reediting and assembly with the user's assembly program. An assembly type output listing can be printed or displayed. The program also outputs files to a storage system tied to the serial control port.

The combined disassembler/trace program allows the user to examine (and execute)—through software single stepping—any memory area including ROM or P/ROM. The disassembler displays program counter, op code, instruction mnemonic, operand, and branch location for relative branches and ASCII characters of valid alphanumeric code. In trace mode, the program displays the CPU status before and after each instruction's execution. The debugging program requires approximately 2300 bytes of RAM.

The relocator takes a program at any contiguous area of memory and relocates it to anywhere in RAM without adjustment. Requiring 952 bytes, this tool also adjusts a program in RAM to operate at another address without actually relocating the program.

The last program is SMITHBUG, a 2k-byte EPROM monitor with 25 commands and debugging functions. It needs an ACIA as the control port and 128 bytes of RAM.

Circle 421 on Inquiry Card

Cross Assembler Allows Use of 6800 μProcessors With MDS Systems

A Motorola 6800/6801 cross assembler for the Intel MDS series of computers operates under the ISIS-II operating system; it uses the standard Motorola mnemonics to symbolize the 6800/6801 instructions. Conditional assembly instructions, cross reference, page width and length controls, and form feed or spacing for new page are all supported. The source statement format is identical to that of Motorola's assembler provided with an EXORciser system, with only a few differences in assembler control statements. It is available on a single- or double-density ISIS-II diskette from Xener Corp, 6641 Backlick Rd, Springfield, VA 22150.

Circle 422 on Inquiry Card

Design Tool Improves Throughput and Uses Resources Efficiently

A realtime, multitasking executive for 8080 and Z80 based microcomputers serves as a system design tool for industrial applications limited by program requirements of realtime interrupt processing, concurrent execution of multiple programs, and sharing of system resources. Under REDX-80™ (Realtime Event Driven Executive) the fundamental program unit is the task; up to 16 user defined tasks can exist concurrently and share system resources. A task with a higher priority level can preempt currently executing tasks to a lower priority.

Tasks are activated or suspended based on stimuli called events, which may be one of the task operations that have occurred. Available task operations include software channel communication for intertask communication, interrupt I/O processing using the hardware channel, and time based requests. A task can identify up to 16 events using event flags.

Users write programs as separate modules that are linked with the REDX-80 object module using link or locate facilities. This module fits in 2k bytes of ROM and requires only 512 bytes of RAM. Systems and Software, Inc, 2801 Finley Rd, Suite 101, Downers Grove, IL 60515, also supplies a set of Macro Libraries. Versions of the executive are available in either Intel ISIS-II relocatable object format or in RT-11/RSX-11M for PDP-11 series computers using a Microbench cross assembler.

Circle 423 on Inquiry Card

Mostek's 16K EPROM. When you need it fast.

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Mostek has established another performance standard with the MK2716 EPROM. Pin compatible with other 5V only 16K EPROMs, it features a fast access time of 350ns (max). From Mostek, you get the high performance and greater design flexibility required in high speed microprocessor systems.

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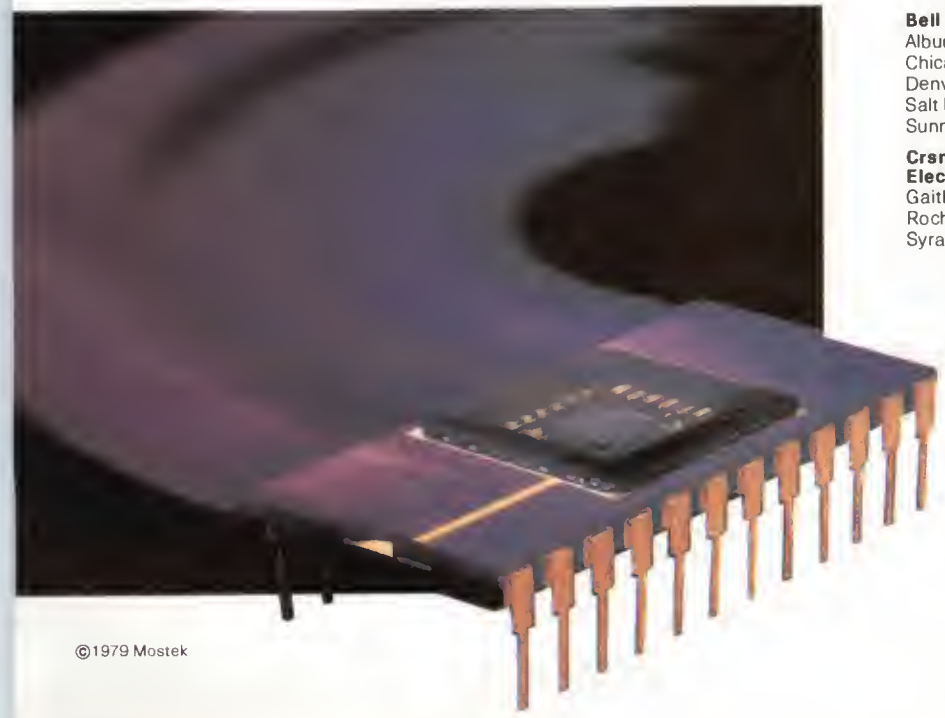
A compatible family. Mostek's Wide-Word Memory Family includes RAM and ROM that are pin compatible with the 2716. All the memory you need, for any system configuration, is available from Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; phone (214) 242-0444. In Europe, contact Mostek Brussels; phone (32) 02/660.69.24.



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☑ Check the Interface
Included at no extra cost, are two input connectors (see photo) that provide three basic ASCII compatible interfaces: EIA Std. RS232C, for interfacing at up to 9600 Baud with most mini-computers and modems; the 20/60 ma current drive mode required by Teletype® ASR33-35 printers; and the parallel-bit, serial character synchronous Centronics compatible interface.

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CIRCLE 85 ON INQUIRY CARD

SOFTWARE

Support Products Aid M68000 Program Development

A cross assembler and simulator, available on magnetic tape, now allow designers to develop and debug programs for the soon-to-be-introduced M68000 microprocessor, using an IBM 360/370 computer. The M68KSAMC cross macro assembler translates source statements written in M68000 assembly language into M68000 machine language. In addition, it is upward compatible with the resident structured macro assembler, which Motorola Microsystems, PO Box 20912, Phoenix, AZ 85036, has scheduled for release with the M68000 development system. Capabilities and outputs include numerous pseudo-operations, conditional assembly capability, macro directives, and assembler output listings.

The M68KEMLC simulator simulates the execution of M68000 machine language instructions in the IBM 367/370 host computer. Although the simulation is not performed in real time, it maintains a count of the simulated execution cycles. The simulator enables testing and debugging of M68000 microprocessor programs in the host computer environment; this eliminates the need for an actual M68000 system during the early development of its software.

Both programs are written in FORTRAN and may be converted to other host computers. Versions of the cross assembler will also be announced for DEC's PDP-11 and the M6800 EXORciser™.

Circle 428 on Inquiry Card

Single-Board Computer Software Provides FORTRAN Capabilities

The iSBC 801™ FORTRAN-80 Runtime Package aids OEMs who, because of system requirements, must execute ANSI Standard FORTRAN application programs on iSBC 80 single-board computers. New FORTRAN-80 programs can be developed or existing FORTRAN software for statistical, industrial, business, scientific, and engineering applications can run on iSBC 80/10, /20, /20-4, or /30 computers under RMX/80™ realtime multitasking software. The software package combined with RMX/80 speeds application program development and shortens product development time. The one-time license fee is $1050.

Comprising a library of programs, the package features compatibility with the RMX/80 software library of control programs as well as with the iSBC 310™ high speed math unit and Intel floating point standard. The formatted I/O feature included by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, allows the format of data entered from an input device or sent to an output device to be specified to appear in integer, floating point, or character form.

The necessary equipment for system generation consists of an Intellec® microcomputer development system with ISIS-II diskette operating system, a minimum of 64k bytes of RAM, dual diskette drives, RMX-80 realtime multitasking executive diskettes, FORTRAN-80 compiler diskettes, and iSBC 801 runtime package diskettes. Using an Intellec system, iSBC 801 routines are linked with user tasks and selected RMX/80 routines to generate a complete iSBC software application system. User tasks may be written in FORTRAN-80, PL/M-80, or ASM-80 programming languages.

Circle 429 on Inquiry Card

Hybrid Program Performs Portions By Assembly Language and BASIC

Advantages of hybrid programs, obtained from the HDS Hybrid Development System for all North Star systems, are higher speed by coding critical segments in assembly language, better protection of proprietary segments coded in assembly language, same execution speed as assembly code while retaining the ease of BASIC program development using internal BASIC routines, and easier performance of certain operations at the assembler level. The system, requiring at least 24k bytes of memory, is available on 5" (13-cm) diskette with documentation for $40.

Allen Ashley, 395 Sierra Madre Villa, Pasadena, CA 91107, has included an interactive assembler/editor to be coresident with BASIC. Modifications made to North Star BASIC Release 4.0 and 5.0 facilitate communication between BASIC and assembly routines. These alterations give access to the addresses of BASIC variables and extend the CALL function to allow an unlimited parameter list. Thus, assembly routines can use BASIC variables or strings and return results to BASIC. A list of BASIC utility entry points and their calling sequence is included in the package.

Circle 430 on Inquiry Card

The intelligent memory for PDP®-11/70's.

More than bits in a box. The MSC 3602 PDP-11/70 add-on memory has its own microcomputer that keeps it, your 11/70 and you out of trouble.

Up to 4 megabytes with single bit error correction and double bit error detection that won't hassle your CPU.

Intelligence speaks for itself. The self-diagnostic microcomputer has RS-232 I/O. No need to interrupt your system. Connect your terminal and the MSC 3602 will speak for itself. You'll know the specific memory addresses which have experienced self corrected one bit errors.

Even without a terminal you can easily view error indications on the front LED display.

Knowing better. The MSC 3602 knows better than to cause a system crash. The microcomputer scans one bit errors from its storage register and decodes them into a usable format. No more need for look-up charts. And error dumps to the terminal can be programmed at any timed interval.

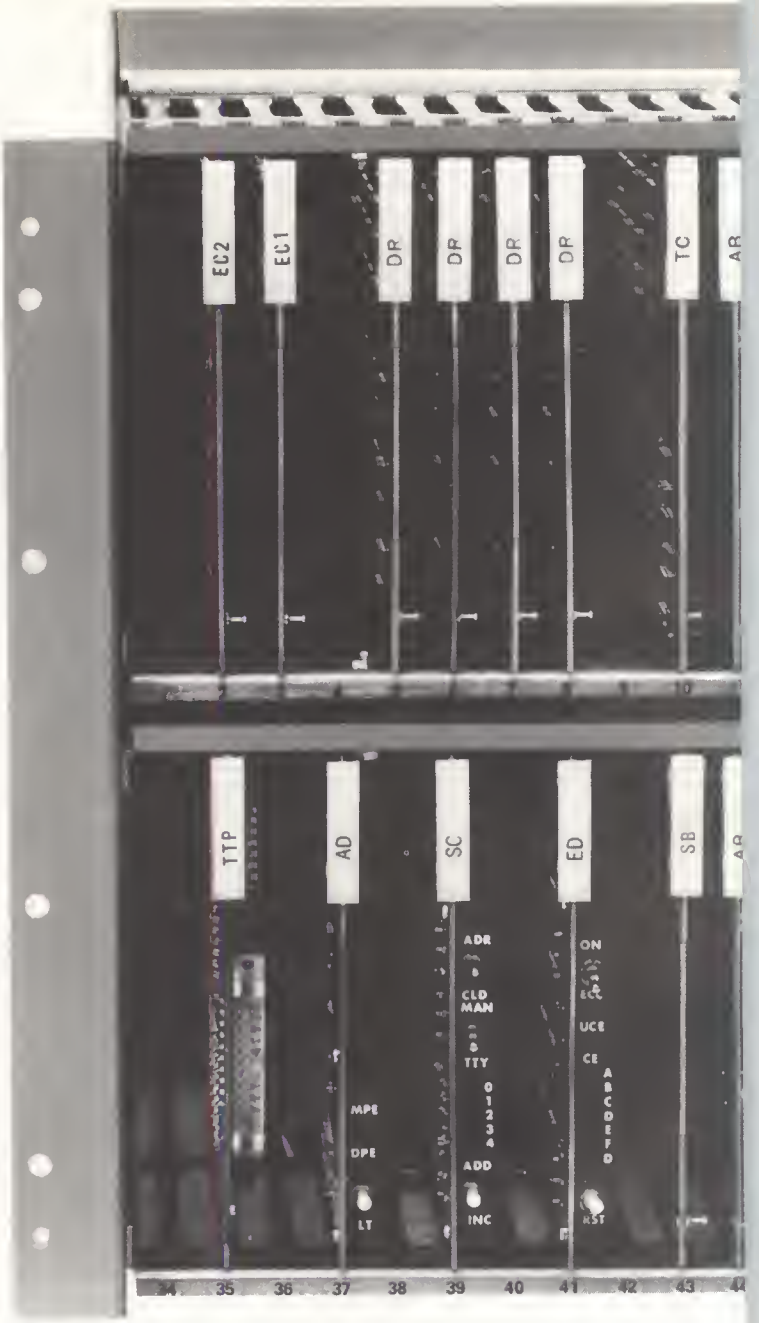
A double bit error causes a parity error message to be sent directly to the CPU.

Turn off the ECC and you can run full diagnostics.

Leaving interleaving. Our intelligent add-on performs at maximum bus speed without using complex interleaving addressing techniques. So, the MSC 3602 is easier to maintain and simpler to manage for you and your 11/70.

Memorizing more? The MSC 3602 will grow with you. It's expandable in 64K byte increments, with 2 megabytes in a single 10½" high free-standing or rackmount chassis including power supply and forced air cooling. An additional 10½" chassis will give you the total 4 megabyte PDP-11/70 maximum memory.

And MOS memory offers you low power requirements. Nonvolatility is available with battery backup.



Intelligent design. The MSC 3602's small size allows close placement to the CPU. Shorter bus lengths allow higher speed and reduce noise problems.

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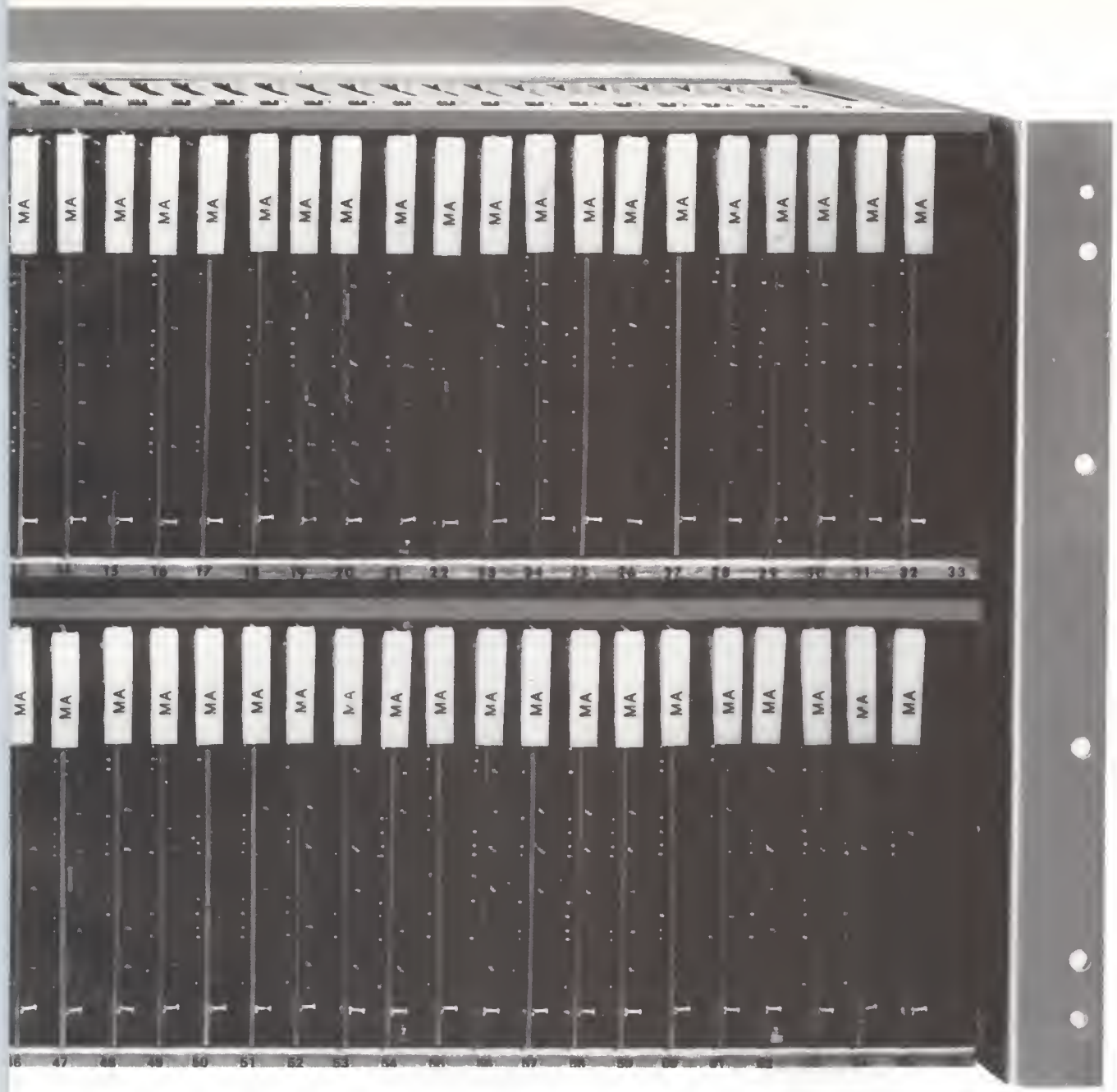

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CIRCLE 86 ON INQUIRY CARD

IMPLEMENTING A DIGITAL FILTER DESIGN IN CUSTOM LSI— REDUCING MULTIPLIER AREA

Lynn Schmidt

Hewlett-Packard Company
Loveland, Colorado

In implementing a digital filter structure in custom LSI, it becomes apparent that some parts occupy more area than others, with arithmetic portions posing the major problem. The basic digital filter building block elements are examined, including their relative sizes in LSI (*Computer Design*, June 1979, p 184), and are shown to result in a chip area too large to be practical. Much of this area is taken up by the requirements of the coefficient multipliers.

A key element in the strategy of designing digital filters in custom LSI is to reduce the total area required by the coefficient multipliers through the use of special arithmetic techniques. Among the modifications that allow sufficient reduction to fit the design on one chip are use of the canonical signed digit method of representing coefficients and restriction of the code to three nonzero bits.

Coefficient Representation

The usual binary coefficients can be represented by the expression

$$X = \sum_{j=0}^{B=1} x_j \, 2^j$$

a weighted sum of B powers of 2, where the weights (x), or bits, can take on the values 0 or 1.

Another method of representing coefficients, called canonical signed digits (CSD), allows the bits to take on the values 0, 1, and $\bar{1}$ (−1). (In the early days of computers, this code was discussed in many publications with reference to fast multiplication.) It has been shown that for any integer X, there exists a unique representation in CSD code in which no two consecutive bits are nonzero.[1] Furthermore, the CSD representation has the least number of nonzero bits. For example, decimal 31 becomes 011111 in binary, or 10000$\bar{1}$ in CSD—only two nonzero bits, compared to five in binary.

CSD representation generally requires 33% fewer nonzero bits than binary. This bit minimization feature is very important in the realization of the LSI filter. Consider the multiplication operation. Although there are many multiplication algorithms, the fundamental technique involves shifting and adding. CSD requires fewer additions than straight binary, because an add is needed only for nonzero bit positions in the multiplier word. Although using a CSD multiplier and a binary multiplicand requires a capability for subtraction, this is just as easy to do as addition. (These techniques result in mathematical operations closely related to the well-known Booth's algorithm for multiplication.) This bit minimization feature, with further improvements, allows the implementation of separate multiplier circuits for each of the 12 coefficients in the filter structure, each occupying a space much smaller than that shown in Fig 2 of last month's column.

Modified CSDs

Further reductions in multiplier complexity are made possible by limiting the number of nonzero bits in each CSD word to three, a representation called "sparse canonical signed digits." While this means that certain values cannot be represented, it is not a severe restriction. Fig 1 shows all the CSD numbers in the decimal range

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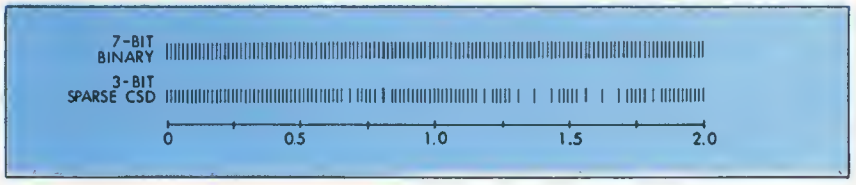

Fig 1 Comparison of discrete values between 0 and 2 available with 7-bit binary code and with canonical signed digital code limited to three or fewer nonzero bits

from 0 to 2 that have three or fewer nonzero bits available, compared to 7-bit binary. (Fractional powers of two are present and restricted to no smaller than 2^{-6}.) An identical set exists for the range −2 to 0. Most infinite impulse response (IIR) digital filters are designed using second order sections having coefficient values between 2 and −2, resulting from the need to keep the poles and zeros on or within the unit circle in the z plane. Thus, very few coefficient values would be missed by using the CSD code restricted to three nonzero bits.

Next there is the problem of designing algorithms for the decimation by 2 and 5 filters using these sparse CSD coefficients. The solution is found by examining the characteristics of a basic digital filter building block—the second order canonic section. Fig 2 indicates the configuration of a second order canonic digital filter section (canonic meaning that this structure has the least number of memory elements with respect to other second order structures, and also involves the least number of multiplications).

Pole and zero locations can be found by substituting all possible sparse CSD values for coefficients a and b in the equations of the z-transform transfer function in Fig 2. The problem is to generate appropriate filter transfer functions using the available pole and zero positions that result from the use of a sparse CSD coefficient value. An iterative procedure can be used. Initially, a prototype analog filter is selected from one of the filter design handbooks. Using the bilinear z-transform, the transfer function H(s) of this filter is converted to H(z). Then with the aid of a computer algorithm, the pole positions of the z-transform are iteratively adjusted to the neighboring sparse CSD positions and the resulting frequency responses are evaluated, the procedure continuing until an optimum response is found.

The preceding technique resulted in finding sparse CSD coefficients for the filter that contain an average of 1.7 nonzero bits. This compares to the four to seven nonzero bits that normally would be required for conventional binary.

Fig 3 shows the resulting block diagram of the filter. Two second order sections are followed by a first order section. The extra multiplier shown at the input serves to multiply the ADC output with the local oscillator output to perform the frequency translation for band-selectable analysis. As shown in the figure, each memory block has eight shift register memories to serve as the z^{-1} (sample) delays for the internal nodes of the filters. The feedback memory collects and saves filter outputs to be used as inputs to the subsequent downstream filter operations in the cascade.

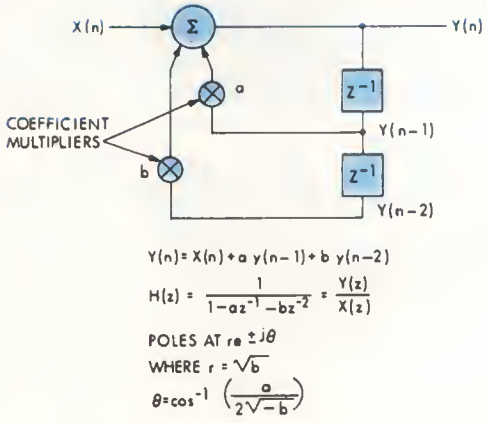

Fig 2 Second order canonic digital filter section. Boxes labeled z^{-1} are storage registers that delay output sample words by one sample period

Details of the design of the basic shift register used in the z^{-1} memories are illustrated in Fig 4. This par-

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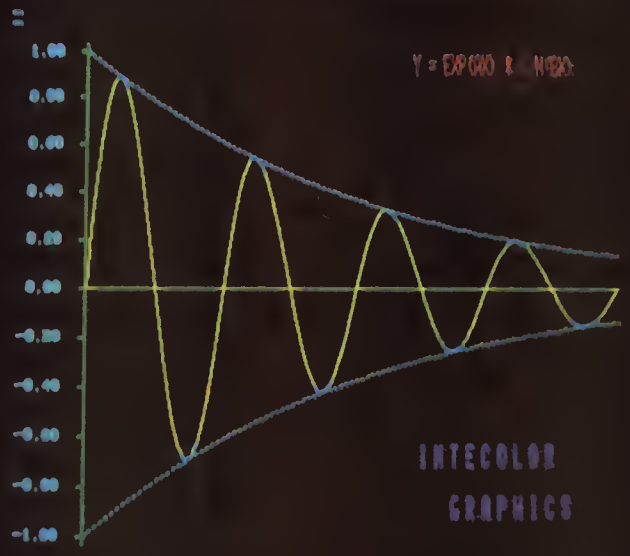

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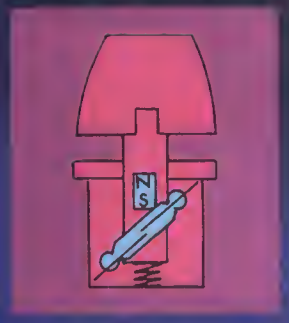

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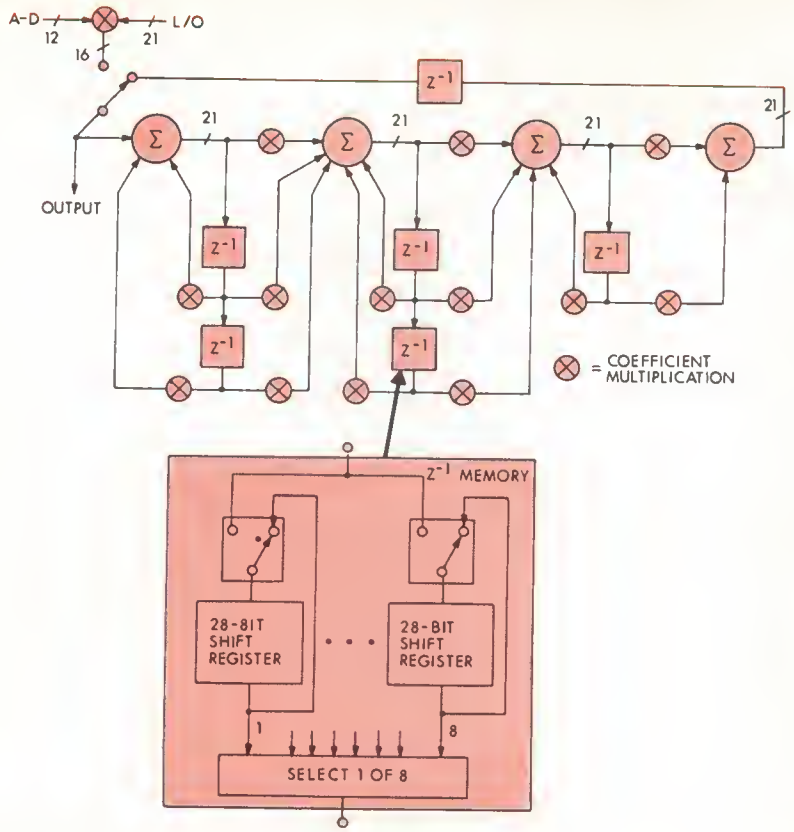

Fig 3 Block diagram of digital filter processor, timeshared by eight different filters in cascade. Eight channels of memory in each z^{-1} block store results from various filter section computations

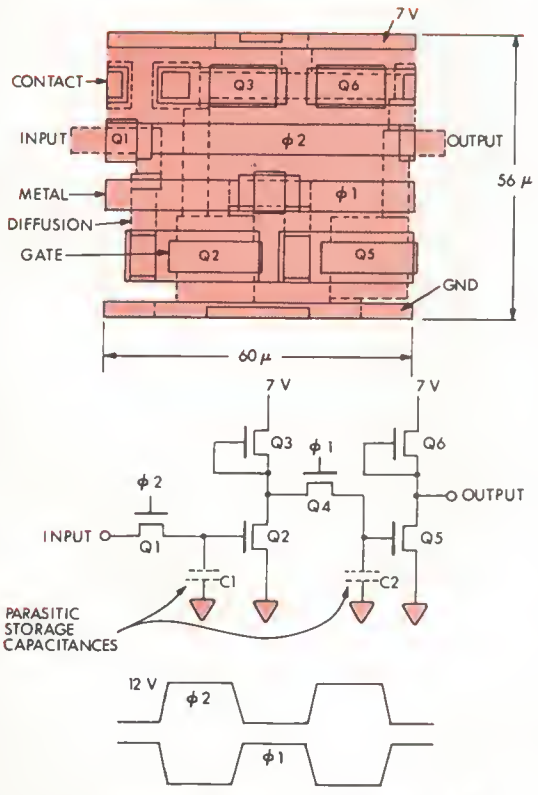

Fig 4 Shift register memory cell used in LSI implementation of digital filter. Bit is stored in parasitic capacitance C1 when clock φ2 occurs, and is transferred to capacitance C2 on clock φ1

ticular cell, called a "ratio design," was selected because of its simplicity and small area, and because it loads the clock lines with less capacitance than other designs. Twenty-eight of these cells are cascaded to form each of the eight circulating shift register memories in each delay element shown in Fig 3. These registers operate at a 6-MHz clock rate.

Summary

In illustrating the nature of designing digital filters in LSI, using the HP 3582A spectrum analyzer as an example,[2] the sparse CSD technique has been proved effective in reducing the chip size to a reasonable area. There are other techniques being used to implement LSI digital filters. One of these offers distinct advantages by essentially replacing the multiplier circuits with read only memory.[1]

The power of digital signal processing available through the use of LSI circuits is now becoming evident in many new fields. An ability to design virtually any arithmetic or memory device needed gives the custom LSI designer new tools to work with, allowing innovative solutions to be used at close to their optimum level. As a cost-effective solution, the use of custom integrated digital filters is already allowing the implementation of functions where the analog approach is impractical to implement.

References

1. A. Peled, B. Liu, *Digital Signal Processing—Theory, Design and Implementation,* John Wiley & Sons, New York, 1976
2. L. A. Schmidt, "Designing Programmable Digital Filters for LSI Implementation," *Hewlett-Packard Journal,* Sept 1978, pp 15-23

Compact 64k CMOS Static RAM Offers Speed and Low Power

The HM5-6564, a miniature array of sixteen 4k x 1 RAMs, occupies a total of 1.8 in^2 (11.6 cm^2) of board space and is claimed to be the first 64k-bit CMOS static random access memory offered in the marketplace. Low power capabilities include a maximum dissipation of 300 mW during operation and 5 mW on standby. The array is organized as two 8k x 4 blocks of RAM sharing only the address bus (Fig 1). Data inputs, data outputs, chip enables, and write enables are separate for each block of RAM. This allows the user to utilize the memory as either an 8k x 8 or a 16k x 4 array. Decoupling capacitors are included to reduce noise and to minimize the need for additional external decoupling.

Applications are found in digital avionics systems, field portable remote data gathering devices, and portable or handheld digital communications systems. The device is appropriate for any application requiring large amounts of RAM operating under small space limitations and consuming very little power.

Each individual RAM in the array is packaged in a leadless carrier (Fig 2). Then, 16 leadless RAMs and 4 decoupling capacitors are reflow-soldered to both sides of a ceramic

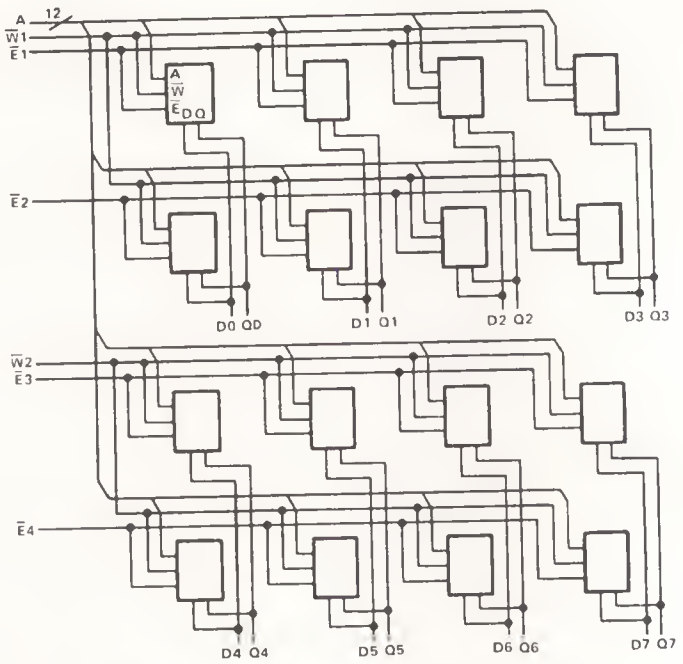

Fig 1 HM-6564 64k-bit CMOS RAM from Harris Semiconductor. Array consists of 16 4k x 1 static RAMs sharing common address bus (A). Write enables ($\overline{W1}$, $\overline{W2}$) each address subset of eight RAMs. Chip enables ($\overline{E1}$, $\overline{E2}$, $\overline{E3}$, $\overline{E4}$) each address four RAMs. Data I/O lines (D0, Q0 through D7, Q7) service one pair of RAMs each

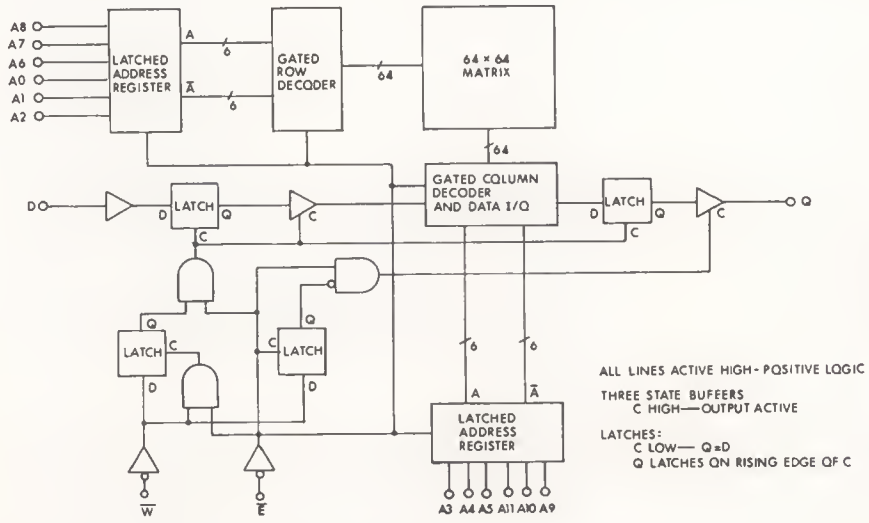

Fig 2 Individual RAM used in array is HM-6504, shown in this logic diagram. 16 of the 4k x 1 CMOS memories, in leadless carriers, are mounted on ceramic substrate. Design emphasizes advanced packaging techniques

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substrate. The substrate is 0.9 x 2.0" (2.3 x 5.0 cm) and has normal side-brazed leads which are plugged into printed circuit boards as in any other dual-inline package. Produced by Harris Semiconductor Group, PO Box 883, Melbourne, FL 32901, the device is offered in a 40-pin DIP.

Utilization of board space for this array can be contrasted to space required for 16 standard 18-pin DIP 4k RAMs. The 16 RAMs would require 12 to 15 in^2 (77 to 97 cm^2) on a standard 2-sided PCB, 9 to 11 in^2 (58 to 71 cm^2) on a fine line or multilayer PCB, and 4 to 5 in^2 (26 to 32 cm^2) on a multilayer alumina substrate. Therefore, the array described here represents a reduction in board space by a factor of at least two and as high as eight.

Other characteristics include a 340-ns access time (max), TTL compatible I/O, 3-state outputs, onchip addressable registers, and data retention to a 2-V minimum. This guaranteed low voltage retention allows easy implementation of nonvolatile read/write memory through use of very small batteries mounted directly on the memory circuit board.

The memory is available in three grades. In the industrial version, the operating temperature range is specified as −40 to 85 °C. Also available are a commercial version (0 to 75 °C) and a military version (−55 to 125 °C).

Absolute maximum ratings limit supply voltage (V_{CC}) to 8.0 V or less, and require that applied input or output voltage lie between ground −0.3 V and V_{CC} 0.3 V. A supply voltage of 4.5 to 5.5 V is within the recommended operating range. Standby supply current is 50 μA (typ), 800 μA (max). Operating supply current is 40 mA (typ) and 48 mA (max) for 8k x 8 operation, these values being halved for 16k x 4 operation.

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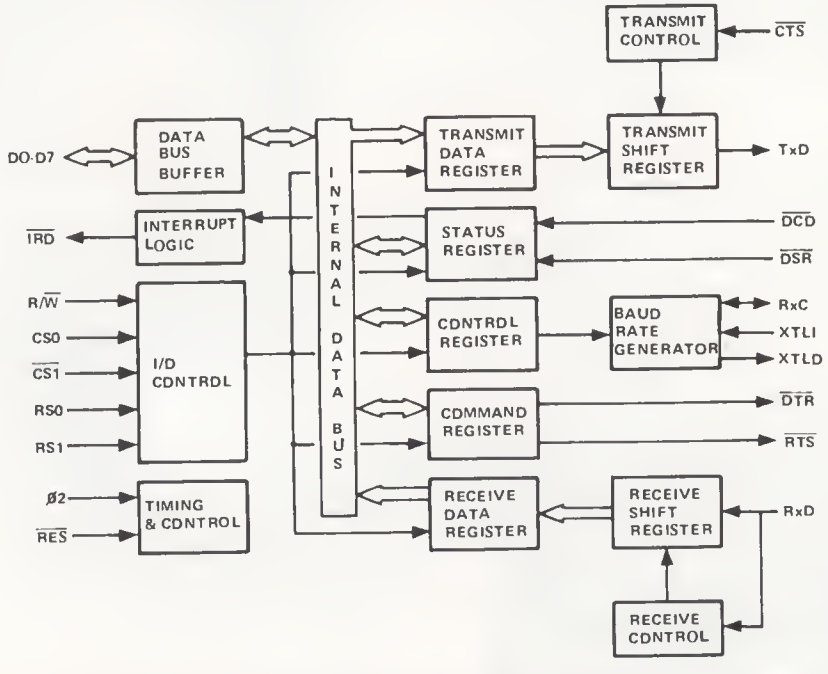

Asynchronous communications interface adapter device, Rockwell's R6551, provides 8-bit microprocessor based systems with UART interface for serial communication to terminals, data sets, and modems. Device is member of R6500 microprocessor family and is also compatible with 6800 based microcomputers

Communications Adapter's Onchip Generator Selects Baud Rates

Providing the interface between 8-bit microprocessor based systems and serial communication data sets and modems, an asynchronous communication interface adapter (ACIA) requires only an accessory crystal to transmit at 15 different program-selectable rates between 50 and 19,200 baud, utilizing an onchip baud rate generator, and receiving at either the transmit rate or at 16 times an external clock rate. The R6551 from Rockwell International, Electronic Devices Div, 3310 Miraloma Ave, Anaheim, CA 92803, has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 start bits.

In addition, the adapter is designed for maximum programmed control from the CPU, to simplify hardware implementation. A control register and a separate command register permit the CPU to select the device's operating modes and data checks easily.

Other features include full-duplex operation with buffered receiver and transmitter, programmable interrupt control, selectable serial echo mode, two chip selects, and full TTL compatibility. The device utilizes a single 5-V power supply and either 1- or 2-MHz clock rate.

Maximum ratings require that supply voltage (V_{CC}) and input voltage (V_{In}) lie between −0.3 and 7.0 V. Allowable operating temperature ranges are 0 to 70 °C for the commercial and −40 to 85 °C for the industrial version, both of which can be stored from −55 to 150 °C. The device is provided in a 28-pin plastic or ceramic dual-inline package.

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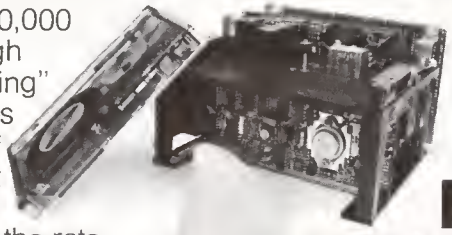

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*Microtape is the DEI name for its 1/4-inch cartridge tape drives.

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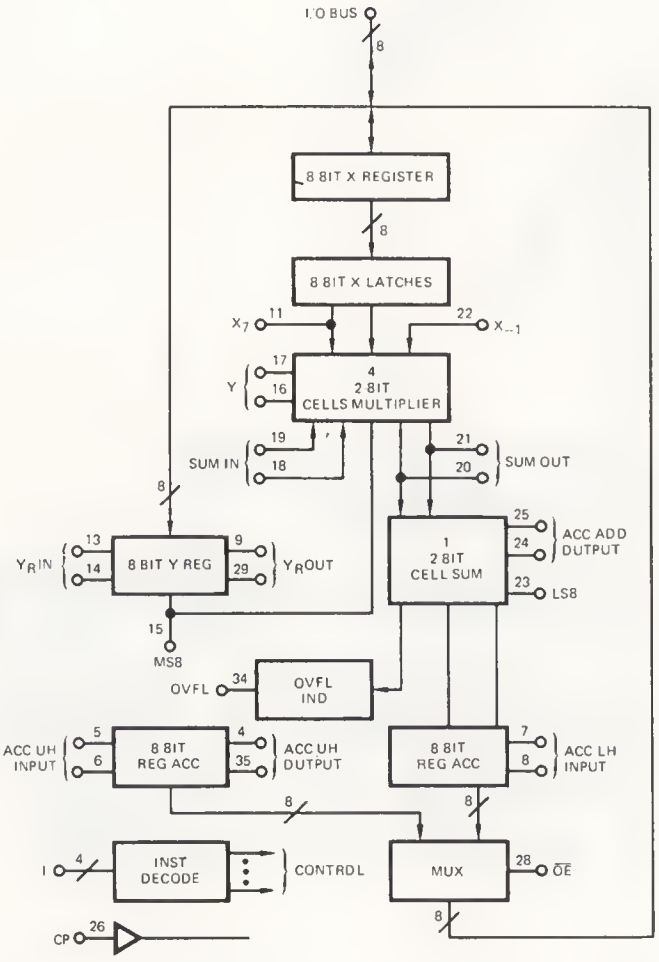

Eight-bit multiplier/accumulator from Advanced Micro Devices. Device includes 8-bit X register prior to X latch providing X hold for chain or overlapping calculations. X and Y registers are loaded with data from bidirectional bus or accumulator register by clocking prior to start of multiply cycle. Double length 16-bit output is multiplexed onto 8-bit bus with either upper or lower half of result readable at any one time

400 ns—eight clock cycles with a 20-MHz clock. Cascading two devices achieves a 16-bit by 16-bit multiplication in only 940 ns over the full military operating range. The low power Schottky device is fully cascadable for use in high speed, realtime signal processing applications such as digital filtering, fast Fourier transforms, and statistical correlation.

Produced by Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086, the Am25LS2516 is externally programmable. It is controlled by 4 instruction lines and responds to 16 microinstructions functionally divided into data moves, reads, and multiplies. These instructions control an 8-bit X-input register (followed by an 8-bit latch), 8-bit Y-input register, four 2-bit multipliers, a 2-bit adder, and 16-bit accumulator.

In operation the X-latch/register combination permits chaining of successive multiplies. Both X- and Y-registers accept data from the 8-bit parallel I/O bus, with the Y-register also able to load from either half of the accumulator. The double length accumulator output is multiplexed onto the 8-bit bus. To simplify cascading, the serial inputs and outputs of the Y-register, low and high order halves of the accumulator, and the 2-bit serial accumulator adder output are available at external pins, both serially and in parallel.

The onchip accumulator minimizes component count and power dissipation in high density systems. For example, it performs an 8 x 8 or 16 x 16 multiplication in only twice the time of parallel multipliers currently available, but uses only one-fourth the power in the multiplier portion of the function and requires no external supporting devices.

This device utilizes 8-bit byte parallel, bidirectional, 3-state I/O bus lines. Other characteristics include onchip registers, overflow indicator, single 5-V supply, and 285-mA (typ) supply current. The parts are 100% screened to MIL-STD-883C requirements, and are provided in 40-pin CERDIPS.

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Gates, Flipflops, and ECL/TTL Translators Are Mil Spec Qualified

MECL 10k JAN-qualified devices are offered by Motorola Semiconductor Products, PO Box 20912, Phoenix, AZ 85036, for all 14 devices listed in the four MIL-M-38510 /060, /061, /062, and /063 specifications. These specifications cover the detail requirements for gates, flipflops, and ECL/TTL translators.

The JAN-qualified devices are manufactured in both dual-inline and flat-pack packages, with either solder-dipped or tin-plate leads, and are available in both Class B and C. A list of the devices includes such examples as a quad OR/NOR gate (MC10501), a triple 2-input exclusive OR/exclusive NOR gate (MC10507), a hex D master-slave flipflop (MC10576), and quad TTL to MECL and MECL to TTL translators (MC10524/25).

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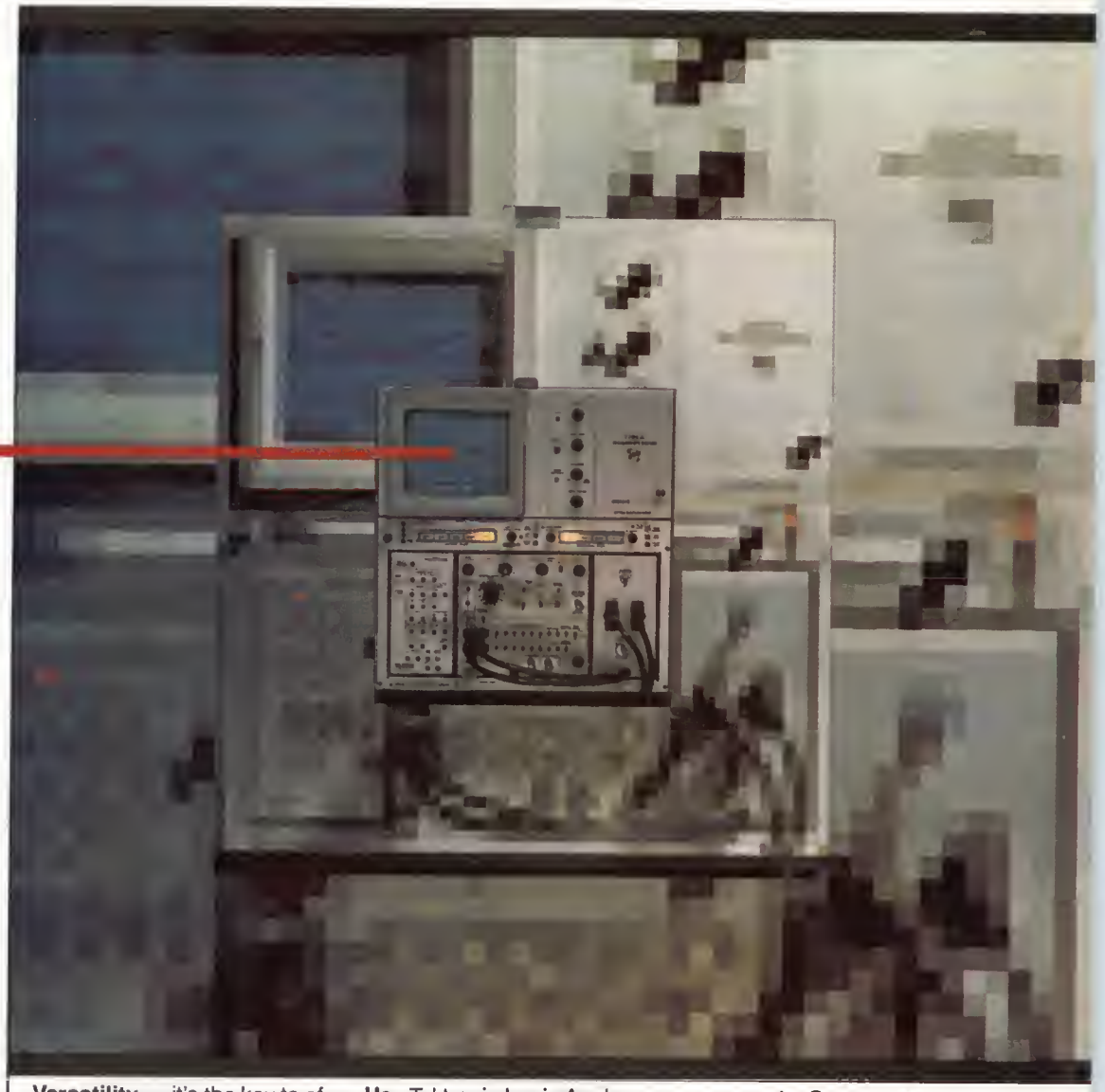

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Line Driver/Receiver Is Designed for Noisy Environments

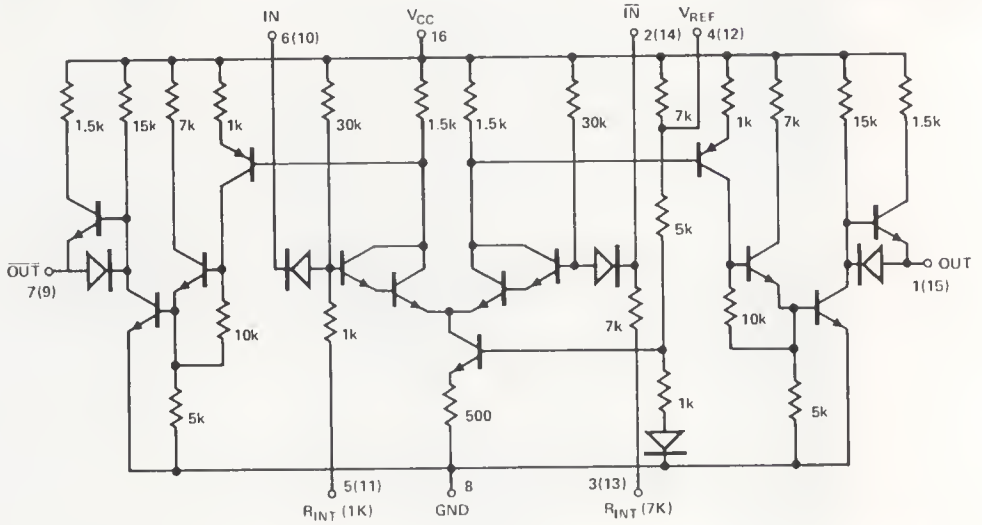
High immunity to electrical noise characterizes a dual differential line driver/receiver designed for use in industrial or other noisy environments, using twisted-pair or single-wire lines. Designated as the 396, this device from Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94043, has an optional built-in hysteresis and reference. The hysteresis capability is very flexible, enabling the designer to adjust the switching thresholds and thus the noise immunity of the device as required. Variation of hysteresis width with changes in power supply voltage is quite linear over the operating range.

A 12- to 15-V power supply operates the device. Rugged bipolar transistors give low output impedance in the high and low states. Low current inputs (0.4 mA) allow direct interfacing with CMOS.

Applications include use as a differential or single-ended line driver or receiver, or as a line repeater. Because of the low frequency operation (<500 kHz), many of the complicated effects associated with line driving and receiving can be ignored and calculations become straightforward. It can also be used as a single-ended slow-down receiver, through connection of a capacitor to the internal 1-kΩ resistor, making the device insensitive to pulses having widths shorter than a predetermined value. The manufacturer further states that it can be used as an alternative to the Motorola MC696.

Absolute maximum ratings limit continuous supply voltage to 16.5 V and pulsed supply voltage (<100 ms) to 18 V. Input voltage must remain between −0.5 and 18 V on any input. The device is supplied in a 16-lead dual-inline package.

Circle 354 on Inquiry Card



Dual differential driver/receiver, model 396 from Teledyne Semiconductor, is designed for industrial logic applications requiring high immunity to electrical noise. System features optional built-in hysteresis and reference

Monolithic CMOS Operational Amplifiers Consume Little Power

A family of very low power operational amplifiers features a 1-pA (typ) input current (in contrast to the 30-pA input currents typical of available JFET input devices), input noise current of 0.01 pA/$\sqrt{Hz}$, and a 10^{12}-Ω input impedance. Low voltage operation is guaranteed at ±0.5 to ±8.0 V, with output swings to within a few millivolts of the supply voltage rails. The monolithic CMOS op amps are capable of single-ended operation from a single NiCd battery.

Intersil Inc, 10710 N Tantau Ave, Cupertino, CA 95014, provides numerous different models within the ICL7611-ICL7642 family. Devices are available as singles, duals, triples, or quads. Other options include internally compensated or uncompensated configurations, extended input common mode voltage to allow the input swing to exceed the supply rails by 0.3 V, and input protection to ±200 V.

A quiescent current selection feature allows the user to program the op amp for standby currents of 1 mA, 100 μA, or 10 μA, using no external components. This results in a power drain as low as 10 μW.

Ac performance of the op amp family also is emphasized by the

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manufacturer. Slew rate is 1.6 V/μs and unity gain bandwidth is 1.4 MHz at $I_Q = 1.0$ mA.

Applications include use in portable instruments, high impedance buffers, and low power replacement for many standard op amps. Because of the low power dissipation, operating temperatures and drift are quite low, leading to utilization in stable instruments, extended life designs, or high density packages.

Manufactured through use of the proprietary MaxCMOS™ process, the amplifiers are provided in TO-99 8-pin cans or 8-pin miniDIPs, or in 14- and 16-pin plastic or ceramic DIPs. Absolute maximum ratings limit total supply voltage (V+ to V−) to 18 V, with neither V+ nor V− more than 18 V from ground. Maximum allowable continuous power dissipation at 25 °C is 250 mW (can or miniDIP), 375 mW (plastic DIP), or 500 mW (cerDIP). Temperatures must stay between 0 and 70 °C for commercial versions and between −55 and 125 °C for military versions, with storage temperature of −55 to 150 °C for all versions.

Circle 355 on Inquiry Card

Low Power MOS RAMs Outspeed Bipolar 1k, 4k Static Memories

Fabricated by a proprietary high density MOS process (HMOS II[R]), a family of static random access memories is more than twice as fast as previous MOS memories of corresponding size. The manufacturer, Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, claims that these are the fastest, lowest power 1k and 4k static RAMs currently available. They are faster than bipolar memories of equivalent storage and use considerably less power. All versions are fully dc stable, requiring no clocks, strobes, or refreshing. Separate data input and output lines are provided, with both input and output having the same polarity. These TTL compatible memories operate from a single 5-V supply.

The 2115H and 2125H are 1024-word x 1-bit random access memories with open collector and 3-state outputs, respectively. These MOS memories may be used to replace bipolar memories in existing product designs, and to enhance performance of future products. Their outputs are capable of sinking a full 16 mA (10 standard TTL loads). Supplied in standard 16-pin cerDIP packages, the units are available in four speeds (suffixes -1 through -4) with maximum access times of 20, 25, 30, and 35 ns over the 0 to 75 °C operating range. Maximum current drain is 125 nA for all units except 30-ns, -3 versions, which have maximum drain of 100 mA.

Uses of 1k static RAMs include cache, writable control stores, and buffer memories—applications where memory speed increases have a significant effect on system performance. This type of application will benefit from the faster 20- and 25-ns memories.

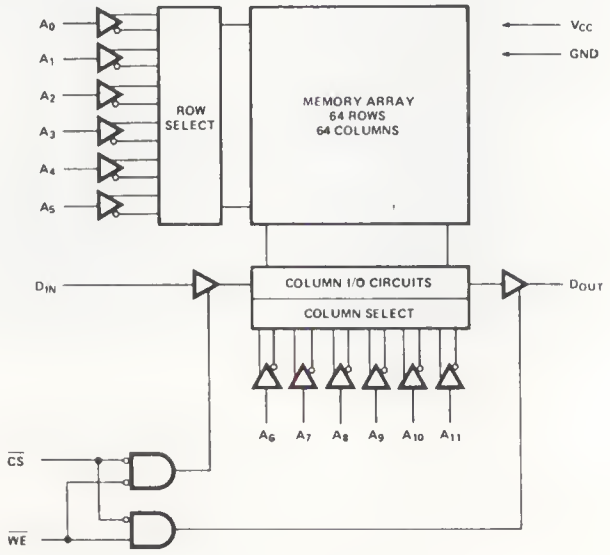
Available in both 35- and 45-ns versions (max access times), the 2147H is a 4096-word by 1-bit random access memory with all the features of the industry standard 2147, at twice the speed. Characteristics include 3-state outputs, a maximum supply current of 180 mA when active and 30 mA on standby, and 18-pin cerDIP housing.

4k HMOS II static memories can be used to increase memory with board space that would otherwise be allocated to 1k RAMs, or to maintain memory capacity and decrease board space. The increased density of these components allows a reduction in both propagation paths and delays, and a corresponding improvement in system performance.

Circle 356 on Inquiry Card

CMOS Multiplying DACs Are Second Sourced

Binary multiplying digital to analog converters employing CMOS technology are being second sourced in 10- and 12-bit models. In each of these



Intel's 2147H 4k-bit static RAM. $\overline{CS}$ controls power down feature, going high to deselect device. Within one cycle time later, memory automatically reduces power requirements and remains in low power standby mode as long as $\overline{CS}$ stays high. This feature results in system power savings as great as 85% in larger systems, where majority of devices are deselected

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CIRCLE 94 ON INQUIRY CARD

models, a deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with a linear error tempco of 0.0002% FS/°C (typ). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low output leakages (200 nA max). Digital inputs are compatible with DTL/TTL levels as well as with full CMOS logic level swings.

A device of this family can be used as a standard DAC when combined with an external amplifier and voltage reference. However, it is also useful for multiplying applications such as digitally controlled gain blocks, since its linearity error is essentially independent of the voltage reference. Other features are a 500-ns settling time, a feedthrough error of only ½ LSB at 100 kHz, and the ability to accept either variable or fixed references over a ±25-V range.

The 10-bit DAC1020 from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, is available with a 10-bit (0.05%), 9-bit (0.10%), or 8-bit (0.20%) nonlinearity and serves as a replacement for the AD7520, AD7530, and AD7533 family. Similarly, the 12-bit DAC1220 provides versions having these same nonlinearities, and replacing the AD7521 and AD7531 family.

BIFET Op Amps Add Options to Existing Families

Low input bias current, low input offset current, output short circuit protection, and internal compensation characterize BIFET operational amplifiers produced by Texas Instruments Inc, PO Box 225012, Dallas, TX 75265. Among the devices that combine these characteristics are the TL061 low power and TL071 low noise families. Now, an op amp offering the option of external compensation has been added to each of these families. Both of the new models have external terminals which allow the designer to tailor the ac response characteristics of the amplifier using standard or feed-forward compensation techniques.

The low power family adds the TL060, which shares the family characteristic of a 0.25-mA (max) supply current. Other features that the device has in common with the family are a 6-mW (typ) power consumption and a 3.5-V/μs (typ) slew rate.

A recent addition to the family of low noise BIFETs is the TL070, featuring a typical equivalent input noise voltage of 18 nV/$\sqrt{\text{Hz}}$. Other family characteristics shared by this device include low harmonic distortion (0.01%, typ) and high slew rate (13 V/μs, typ).

Following shortly after the introduction of the preceding two devices, the same manufacturer announced a dual version of the existing TL087 BIFET operational amplifier. Designated the TL287, the dual op amp has the same low input offset voltage as the single amplifier, guaranteed at 0.5 mV (max).

Each of the op amps described here also features high input impedance, JFET input stage, and wide common-mode and differential voltage ranges. They are available in models specified for either military or commercial temperature ranges, in 8-pin ceramic or plastic dual-inline packages.

Circle 357 on Inquiry Card

IC Generates 12-Point Fluorescent Bar Graph Display

A 12-point level-detector IC, designed for interfacing with fluorescent displays, consists of an input buffer amplifier, 12 high gain comparators, an internal voltage reference, and a bias-setting resistor string. The XR-2276 from Exar Integrated Systems Inc, 750 Palomar Ave, Sunnyvale, CA 94088, is especially suited for generating 12-point bar graphs or other multisegment fluorescent displays.

All comparator stages have independent buffered outputs and each has a threshold level higher than the preceding stage. With no input signal, all of the comparators are off and all outputs are low. As the input level is increased, the outputs successively switch to high, at 12 discrete input levels. These threshold levels are set within the range of −20 to 8 dB, referenced to an externally adjustable 0-dB level setting.

The device features high input impedance, internal pull-down resistors, logarithmic display characteristics, and external reference level adjustment. It can function as a 12-point sequential controller, level detector, or channel separation indicator, and offers a wide range of applications in dot matrix or alphanumeric displays.

Absolute maximum ratings limit the power supply to 24 V, output current to 5 mA, and power dissipation to 625 mW, derated above 25 °C by 5 mW/°C. The input signal must lie between −1 and 10 V. Temperature is constrained to the 0 to 75 °C range during operation and the −65 to 125 °C range in storage. The device is provided in a 16-pin dual-inline plastic package.

Circle 358 on Inquiry Card

Single-Chip Pulse Detector Offers Low Threshold

A single-chip pulse detector consists of a fast input preamplifier, which can be ac-coupled through external filter or waveshaping networks to a biased voltage comparator. Threshold sensitivity, referred to the input, is externally voltage programmable from 150 μV to 2.4 mV. Hysteresis is 75 μV and power dissipation is only 0.5 W.

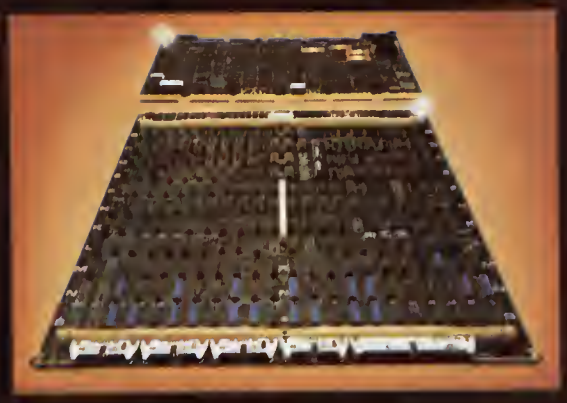
Designed for the detection of low level pulses, the MVL100 from LeCroy Research Systems Corp, 700 S Main St, Spring Valley, NY 10977, offers a threshold of ±200 μV (typ) and time slewing of 1.5 ns from 2X to 20X threshold. Adjustable from less than ±250 μV to greater than ±3.2 mV, the threshold has stability of <0.2%/°C.

Differential input connectors reject common mode noise and offset up to ±1 V. The output element is a nonretriggerable multivibrator externally adjustable from 20 to 1000 ns by selection of RC timing components. Outputs are standard ECL levels which switch between −0.8 and −1.6 V and can drive separate 50-Ω loads or a 100-Ω twisted pair. The device is provided in a 16-pin DIP.

Circle 359 on Inquiry Card

MiniComputer Technology

The solid name in disk controllers introduces two smart new single boards. For DEC and Data General.



Above, the SMC11 (DEC)

Below, the SMC 12 (DG)

They're ready for delivery now. Intelligent storage module disk controllers with multi-drive capability, multiple sector transfer, and hardware error correction. They come complete with cables and manuals. For $3580, quantity one.

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Interdata people, ask about the SMC903.

CIRCLE 95 ON INQUIRY CARD

2k x 8, 4k x 8, and 8k x 8 Quasistatic RAMs, Are Second Sourced

Second source and standardization agreements have been reached concerning a family of quasistatic 8-bit wide random access memories. Zilog Inc, 10340 Bubb Rd, Cupertino, CA 95014, and National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, have jointly agreed to specifications conforming to the proposed JEDEC 28-pin configuration, for the three functionally and electrically compatible devices.

National is to receive tooling and technical information for Zilog's recently announced 4k x 8 quasistatic RAM, the Z6132. The 2k x 8 version will be a subset of the 4k x 8. For the 8k x 8 memory, National in cooperation with Zilog has configured the pinouts, and functional and electrical characteristics of its design (the National NMC 4864 and Zilog 6164) to be compatible with Zilog's family of microprocessors (including the Z8000), with National's 16000 processor, and with other advanced CPUs.

This agreement is expected to facilitate standardization of high density, quasistatic RAMs in byte-wide configurations, with availability from multiple sources in standard pinouts accelerating adaptation to system designs. The technology is intended to provide users with the high density integration of dynamic RAMs and ease of use of static RAMs.

Zilog plans to sample the Z6132 this summer with production a few months later. National plans to sample the Z6132 in the third quarter with production in the fourth quarter. Samples of National's NMC 4864 will be available in the fourth quarter this year with production in the second quarter of 1980. Zilog has scheduled samples and productions of the Z6164 (8k x 8) device in the second and third quarters of 1980, respectively.

4-Digit CMOS IC Decodes and Drives Liquid Crystal Displays

A CMOS integrated circuit, operating as a liquid crystal display (LCD) driver, contains all the circuitry needed to decode up to four digits of multiplexed BCD information and derive the ac signals needed to drive a 4-digit LCD display. All inputs are CMOS, NMOS, and TTL compatible. Several of the devices may be cascaded for larger displays.

The SCL25411, produced by Solid State Scientific Inc, Montgomeryville, PA 18936, comes in a 40-pin plastic or ceramic package. Included in the circuit is an onboard oscillator (it is frequency controlled by an external capacitor), which develops a backplane signal that is a square wave swinging between ground (V_{SS}) and the positive supply (V_{DD}). Segment drivers supply square waves of the same frequency as the backplane but either in phase for an off segment or out of phase for an on segment. In this manner of LCD digit driving the net dc voltage applied between segment and backplane is zero, a necessary requirement for long display life. Digital input levels are defined as input voltages >5 V being a logic 1 and input voltages <0.8 V being a logic 0, with V_{DD} equal to 6 V.

Absolute maximum ratings require that $V_{DD} - V_{SS}$ lie between −0.3 and 8 V and that the voltage on any pin lie within V_{SS} −0.3 V and V_{DD} 0.3 V. Current on any pin may not exceed 10 mA, nor may the power dissipation go above 450 mW. The allowable temperature range is 0 to 70 °C during operation and −65 to 125 °C in storage.

Circle 360 on Inquiry Card

Monolithic IC Corrects CRT Focus Geometry

A circuit that is claimed to be the industry's first monolithic geometry and focus corrector replaces complex diode breakpoint circuits, large and expensive discrete modules, and complex multiplier schemes. This device from Intronics, 57 Chapel St, Newton, MA 02158, is designed to provide a cost-effective solution to distortion in CRT displays by giving the user single-chip reliability along with the flexibility to adjust for different tube geometries and system types. Possible applications include high precision alphanumeric and hybrid displays; CRT displays for mapping, plotting, and computer aided design; computer generated graphics displays; computer output microfilming; and closed-circuit TV systems.

Available in five different models, the C310 series comes in a 16-pin DIP, while the C410 series is a 24-pin DIP. For a 50° total reflection angle, the C310, C311, and C312 are accurate to 2%, 1%, and 0.5%, respectively. The C410 is 1% accurate and the C411 is 0.5% for the same 50° angle.

Circle 361 on Inquiry Card

32k ROM Provides Both Standard JEDEC Pinouts

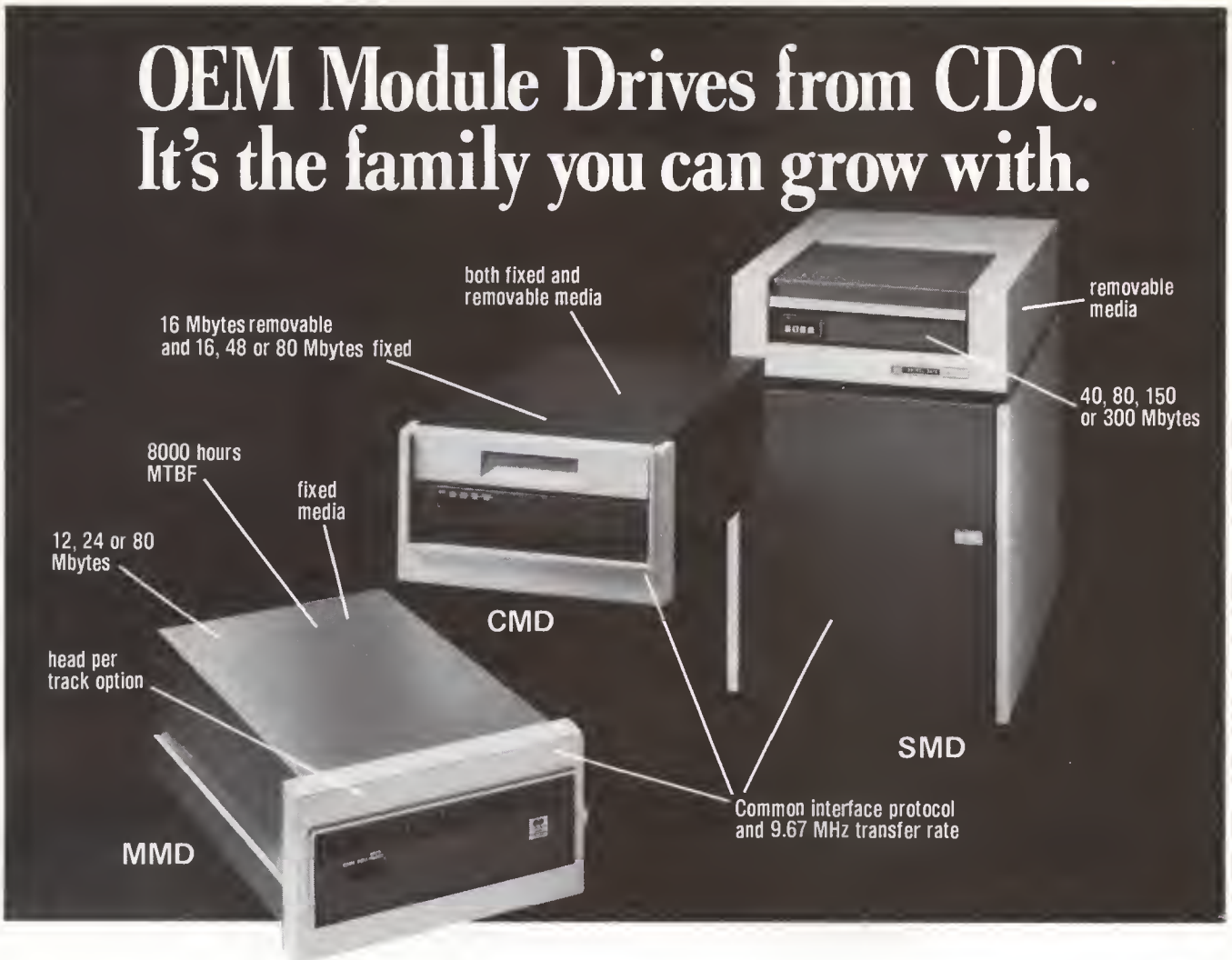
A 32k-bit fully static read only memory, utilizing NMOS silicon-gate ion-implanted technology, offers either of the two JEDEC standard pin configurations as program options. The EA-8332 from Electronic Arrays Inc, 550 E Middlefield Rd, Mountain View, CA 94043, is organized as 4k words x 8 bits and operates from a single 5-V power supply with ±10% tolerance. All inputs are TTL compatible, and the 3-state outputs can drive two standard TTL loads each.

The memory is available with a maximum access time of either 450 or 350 ns. Other features include two programmable chip select inputs, pin compatibility with EA2716 and 2732 EPROMS, and all inputs protected against static charge. Contact mask programming results in a 3-week turnaround of first samples.

Absolute maximum ratings require that voltage on all inputs, outputs, and supply pins lie between −0.5 and 7.0 V. Typical power supply current is 60 mA, with a maximum of 90 mA. The devices are packaged in 24-pin molded or hermetic DIPS.

Circle 362 on Inquiry Card

OEM Module Drives from CDC. It's the family you can grow with.



Control Data offers you a *family of module drives* because OEM storage requirements vary. One application may demand the high capacity and removable media offered by our Storage Module Drive (SMD). Another application may demand the exceptional reliability and fixed media of our Mini Module Drive (MMD). Or maybe our Cartridge Module Drive (CMD) with both fixed and removable media best fits your application.

But there's one thing that our SMD, MMD and CMD all have in common. All feature the widely accepted 9.67 MHz transfer rate. All use compatible interface software and firmware. That means you don't have to change your basic design every time your storage requirements change. That means easier system integration and simple field upgrades. And one source for all your storage requirements.

One Source and One Standard of Excellence

These module drives share something else that's important to an OEM. Quality. We design and manufacture all critical components in-house. We can build reliability into our drives because we built it into our heads, servos and media. Control Data has earned a reputation for building equipment that lasts.

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CIRCLE 96 ON INQUIRY CARD

PRODUCT FEATURE

Flexible, Low Cost OEM Printers Meet Small Business System Needs

Text printer requirements that do not demand the sophistication of high priced printers but that cannot be satisfied by low level hobby units are met by the Dataroyal IPS-5000 family. These serial and parallel interface impact printers feature the versatility of microprocessor control yet have an OEM price comparable to that of hobbyist models. They are designed for use with either mini or microcomputers, for CRT terminal hardcopy output, or as message receiving printers.

Features and Capabilities

Control of each printer is maintained by a single-chip F8 microprocessor, with associated random access and programmable read only memories on one printed circuit board. Dot matrix and software changes are made by replacing a chip. Stepping motors individually drive the ballistic type printhead and the tractors.

The printer can generate a 96 ASCII character set with true lower case descenders bidirectionally at 150 char/s in a 9 x 9 dot matrix. Features include 256-char buffer, pin feed tractor drive for fanfold paper 1.5 to 10″ (3.8 to 25.4 cm) wide, 0.25″ (0.6-cm) 18-yd (16-m) nylon fabric ribbon in a continuous loop cartridge, and 6-part form capability. The unit has a 256-char buffer and short line printing capability. Paper feed can be from either front or bottom.

Top of form control, selectable expandable characters, 10-char/in (4/cm) and 6-line/in (2.4/cm) spacing, 5-in (12.7-cm)/s paper slew, front panel controls and indicators, and heavy duty construction are standard. Character height is 0.105″ (0.267 cm) high by 0.075″ (0.19 cm) wide. RS-232 interface, 100- to 9600-baud communications capability, TTY level 8-bit parallel current loop interface, and expanded buffer are optional features. In addition to English, foreign character fonts will be available in Swedish, Danish, Italian, and German. Both 80- and 132-char/line versions are available as standard units.

Electrical and Environmental Specifications

Voltage requirements are 100 Vac, 60 Hz or 220 Vac, 50 Hz, at 150 VA power. Operating temperature range is 5 to 35 °C (41 to 95 °F), 10 to 90% relative humidity.

Price and Delivery

80-col versions of the IPS-5000 printers sell for $925 in single quantity and $625 each in 100 quantities. The 132-col version sells for $995 in single and $725 in 100 quantities. Deliveries for both are 90 days ARO. Dataroyal, Inc, 235 Main Dunstable Rd, Nashua, NH 03060. Tel: 603/883-4157.

For additional information circle 199 on inquiry card.

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When it comes to static RAMs, think Synertek. We're experts.

For specs, samples and complete information, contact your local Synertek distributor, sales representative or Memory Product Marketing, Synertek, Inc., 3001 Stender Way, Santa Clara, California 95051. (408) 988-5611. TWX: 910-338-0135.

Synertek sales affices: **Eastern Region,** 400 Humphrey St., Suite 2, Swampscatt, MA 01907 (617) 595-1170; **Central Region,** 4615 W. Streetsboro Rd., Suite 204, Richfield, OH 44286 (216) 659-4195; **Midwest Region,** 2805 Butterfield Rd., Suite 150, Oakbrook, IL 60621 (312) 986-8989; **Western and Northwest Regions,** 20863 Stevens Creek Blvd., Bldg. B3, Suite C, Cupertina, CA 95014 (408) 255-3941; **Southwest Region,** 1000 Quail St., Suite 290, Newport Beach, CA 92660 (714) 752-5535; **Europe,** Haneywell Hause, Charles Square, Bracknell, Berkshire, England, Rg 12 1Eb. Direct Dial: 011-44-344-24555.

Part Number	Speed	Pawer	Organization	Package
SY2114	200-450nsec	500mW	1024x4	18 pin
SY2114L	200-450nsec	350mW	1024x4	18 pin
SY2114LV	200-450nsec	350mW	1024x4	18 pin
SY2142	200-450nsec	500mW	1024x4	20 pin
SY2142L	200-450nsec	350mW	1024x4	20 pin
SY2142LV	200-450nsec	350mW	1024x4	20 pin
SY2101A	250-500nsec	275mW	256x4	22 pin
SY21H01	175-200nsec	450mW	256x4	22 pin
SY2111A	250-500nsec	275mW	256x4	18 pin
SY21H11	175-200nsec	450mW	256x4	18 pin
SY2112A	250-500nsec	275mW	256x4	16 pin
SY21H12	175-200nsec	450mW	256x4	16 pin

Off-The-Shelf Delivery Fram These Synertek Distributars:

Arraw Electronics
Kierulff Electronics
Sterling Electronics
Zeus
Century/Bell
Sheridan Sales
Technico
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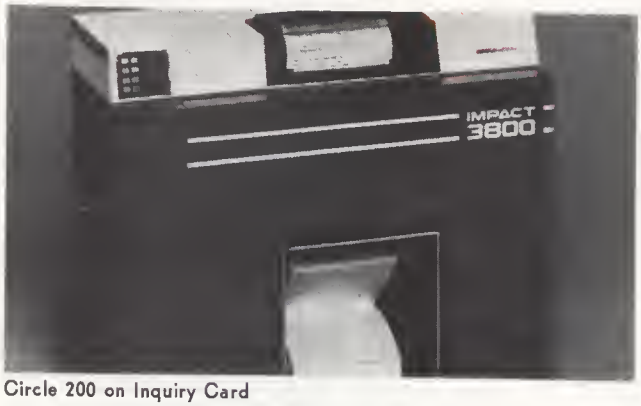
Aiiiance Electranics
Parratt Electronics
Western Microtechnoiogy
Summit Distributors
Lianex
Hall-Mark
intermark Electronics
Advent Electronics
Quality Components
Taylar Electric
Future Electranics
Emitter Electronics
R-M Electranics

SYNERTEK, INC.
3001 Stender Way, Santa Clara, California 95051
(408) 988-5600. TWX: 910-338-0135.

CIRCLE 97 ON INQUIRY CARD

PRODUCTS

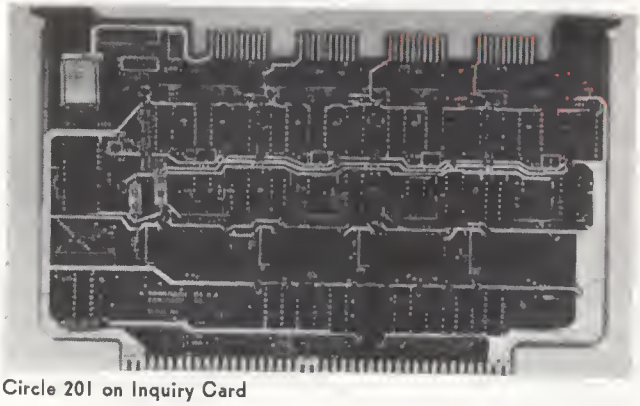
Impact Line Printer Advances Produce Speeds of 3800 Lines/Min



Circle 200 on Inquiry Card

Offering impact printing at nonimpact speeds, the IMPACT 3800 enables the user to print up to 6-part forms. Throughput is enhanced with a slew rate of up to 100 in (254 cm)/s. The unit can print 57 std 11 x 14 pages (150- or 132-char lines) at 6 lines/in (2/cm) in 1 min, which is equivalent to 9500 char/s. Changes in hammer striker technology have reduced the hammer-duty cycle to less than 6 ms. The printer measures 60 x 29 x 53" (152 x 73 x 134 cm) and weighs 1300 lb (590 kg). Interchangeable char sets consist of 48-char commercial and scientific, 63-char PLI and ASCII, and 87-char text. Electrical requirements are 208/230 Vac line to line, 50 or 60 Hz, 3-phase (4-wire), wye connected. A low inertia tractor system provides faster paper movement. A microprocessor controller communicates with the host, decodes commands, controls the printer, and reports various error and status signals. **Documation Inc,** PO Box 1240, Melbourne, FL 32901.

System Module Communicates In Distributive Serial Mode



Circle 201 on Inquiry Card

Multiple communications channels are available on a single board with the M68MM07 Quad Communications Micromodule. Together with a microcomputer module, this device allows a system to communicate with other multiple systems. Each of the 4 communications channels has separately configured electrical interfaces for use of all serial interfaces. Each port is strappable as RS-232-C or -423, RD-422, or 20-mA current loop. MC6850 ACIA devices are used in the std configuration; each adapter has separate transmit and receive rates with 21 buffered baud rates, jumper selectable from 75 to 11k. A user may install MC6852 synchronous serial data adapters for mixed applications. Operating at 1 MHz, the module is EXORciser™ and Micromodule compatible. It is bus buffered and accommodates dual or multimap systems. Odd, even, or no parity, and 1 or 2 stop bits are program selectable. **Motorola Microsystems,** PO Box 20912, Phoenix, AZ 85036.

OEM Winchester Disc Drive Offers Medium Capacity, Low Cost Storage

DISKOS 3350 uses a fully servoed voice coil positioner to achieve a capacity of 33M bytes on a single 14" (36-cm) disc. The 7 x 17.5 x 20" (18 x 44.5 x 51-cm) drive is aimed at small business computer, word processing, and communication systems. A brushless dc spindle drive motor eliminates the mechanical brake and permits the unit to be used in systems requiring all dc power. A microprocessor controls head seek operations and sequencing of power in the drive, and performs diagnostics and self-test. An internal air filtering system and breather filter design prevent contamination of the system by external air, even if the head-disc cavity seals were to leak. The drive weighs 33 lb (15 kg). An optional power supply can be included in the drive envelope. **Priam Corp,** 20730 Valley Green Dr, Cupertino, CA 95014.

Circle 202 on Inquiry Card

C. Itoh's Model 8300 printer looks superb.

It works even better.

C. Itoh offers you the perfect OEM printer for general purpose computers, communication terminals, data loggers and micro computers: the Model 8300. This quiet and low-cost unit features a straightforward, reliable design and a continuous-duty 7-wire head with a life expectancy of 100 million characters. Designed with a 7-bit parallel interface, the 80-column, dot matrix Model 8300 prints bi-directionally at 125 CPS. Its sprocket paper feed mechanism accepts multi-ply pin-feed paper in any width from 4.5″ to 9.5″; paper can be loaded from the bottom or rear; and print line position is readily adjustable. The Model 8300 works even better than it looks. Would you expect anything less from C. Itoh? Write today for detailed specifications.

C. Itoh Electronics, Inc.

C. Itoh means excellence in printers.

5301 Beethoven Street, Los Angeles, CA 90066
Call: (213) 390-7778 • Telex: WU 65-2451
East Coast
280 Park Avenue, New York, NY 10017
Call: (212) 682-0420 • Telex: WU 12-5059

C. Itoh Electronics is part of the 119-year-old C. Itoh & Co., Ltd., world-wide trading organization.

CIRCLE 98 ON INQUIRY CARD

Look What's Happening at Teleray!

Teleray is on the move in smart terminals. Our list of satisfied users is gowing rapidly, and for good reason. These terminals are:

- **ESPECIALLY SMART** — 32 programmable keyboard functions, full editing, formatting and tabular control, interactive and block mode communication.
- **APPLICATION DESIGNED** — Available in APL (true overstrike), or as DEC, DG or Microdata replacements . . . together with Teleray "intelligence".
- **PACKAGED TO SUIT** — Attractive Model 10 format for "front office" use, Model 1061 for rugged day-to-day use in any environment, and Model 10-R for standard equipment racks.
- **INSTANTLY SERVICEABLE** — Replace snap-in logic, power, monitor or keyboard modules in seconds, no tools, no down-time. Reusable mailers make service fast and simple.

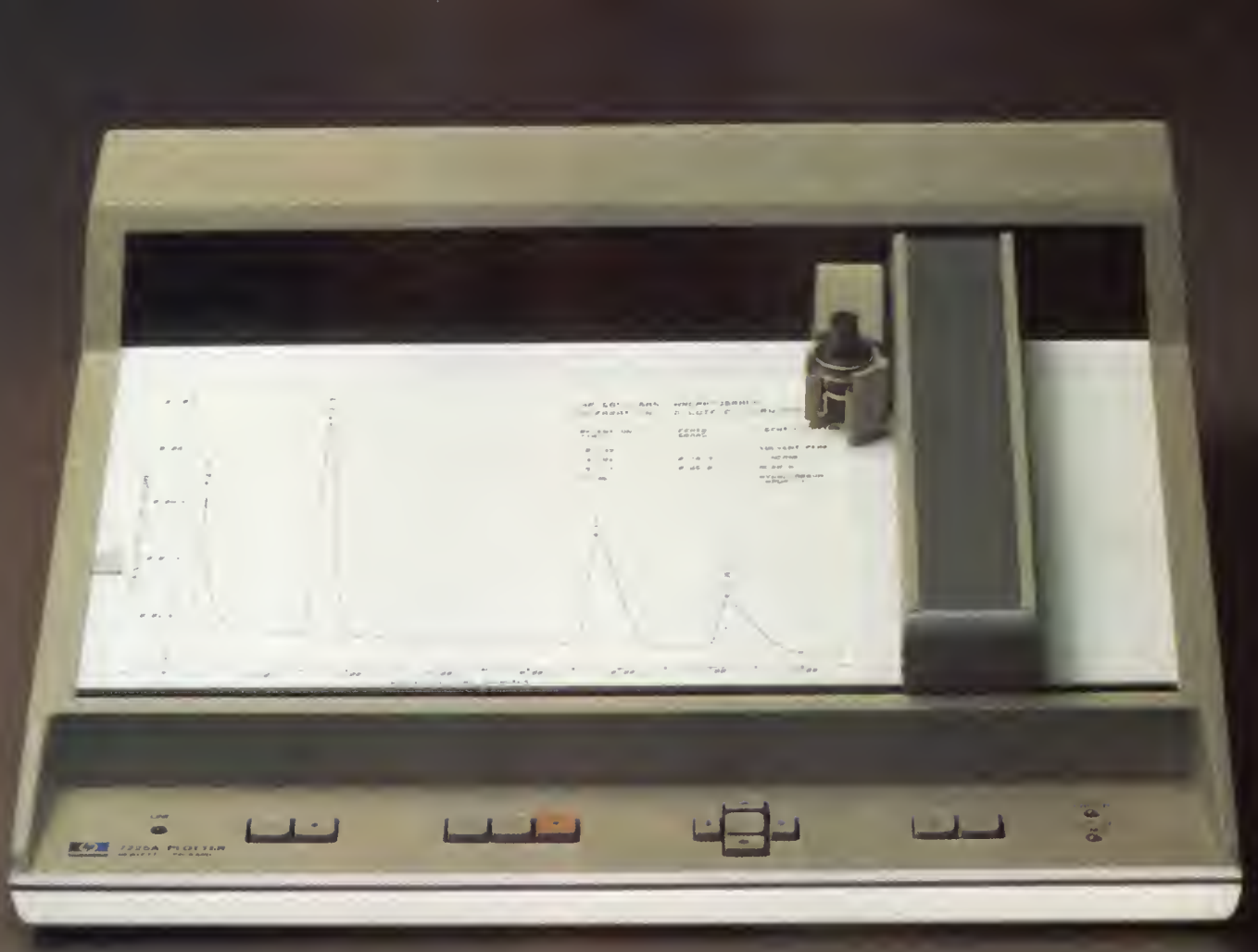
Teleray terminals have the lowest price/performance ratio in the business. Be a part of what's happening in smart terminals. Look into Teleray!

TELERAY DIVISION OF **RESEARCH INC**

BOX 24064 MINNEAPOLIS, MINNESOTA USA 55424
PHONE (612) 941-3300

(201)652-7055	(206)641-6444	(215)723-8733	(303)279-7796	(313)354-6421	(412)243-8421	(513)223-8421	(617)459-2578	(716)381-4120
(201)944-1600	(212)947-0379	(216)585-8421	(305)421-4989	(404)955-0293	(503)292-3505	(518)587-2313	(713)780-2511	(801)969-4034
(203)623-5352	(213)328-9770	(301)589-2802	(305)645-3444	(405)528-6071	(512)451-5174	(602)968-5962	(714)273-4771	(808)523-1326
(205)881-9298	(214)661-0300	(301)828-8928	(312)655-0040	(408)744-1930	(512)828-0937	(612)535-5330	(714)552-7850	(919)883-9125

CIRCLE 150 ON INQUIRY CARD



Now OEM's can draw high quality graphics even when the bottom line is price.

Graphics gives you the best way to analyze and communicate data. But cost has been keeping it out of the picture for many OEM systems. That's why Hewlett-Packard is offering the new Model 7225A Graphics Plotter.

The price: $1750 (domestic USA price with 17602A general purpose "personality" module), in quantities of five. With further OEM discounts from there.

Plug-in "personality modules" customize the plotter for you.

HP's versatile 7225A converts the output of processor based systems into high quality charts and graphs in any size up to 8½ x 11" (A4). A wide selection of plug-in "personality modules" lets you adapt the plotter to suit your needs. Different modules determine interface hardware, language, and capabilities such as internal character sets, axis generation, labeling and scaling.

Simple linear stepping motors eliminate many moving parts to assure reliability. Visually smooth, high resolution ink lines of any length and angle are generated, requiring only end point data.

And you give your customers the confidence of Hewlett-Packard's worldwide service network.

So if you want high quality graphics but you draw the line at price, look into the Model 7225A Graphics Plotter. For a detailed 24-page OEM brochure, contact Hal Phillips at Hewlett-Packard, 16399 West Bernardo Drive, San Diego, CA 92127; (714) 487-4100. 11901

HEWLETT hp PACKARD

1501 Page Mill Road, Palo Alto, California 94304

For assistance call: Washington (301) 948-6370, Chicago (312) 255-9800, Atlanta (404) 955-1500, Los Angeles (213) 877-1282

CIRCLE 25 ON INQUIRY CARD

PRODUCTS

RS-232 DUAL-CASSETTE TERMINAL

A Motorola 6800 microprocessor and 2 model 6406 cassette drives comprise the model 6801 terminal which reads, writes, or copies data in ANSI X3.48-1977/ECMA34 format; it can also be switched to a format compatible with existing TI terminals. The serial, full-duplex RS-232-C or current loop interface is switch selectable in 8 steps for data transfer rates of 110 to 9600 baud. It emulates punched paper tape and will function with PDP-8 or -11 operating systems in this mode. **Raymond Engineering Inc, Raycorder Products Div,** 217 Smith St, Middletown, CT 06457.

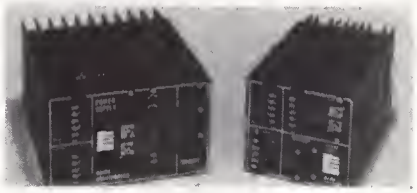
Circle 203 on Inquiry Card

14-BIT S/H AMPLIFIER

High sampling rates up to 50 kHz are obtained in 14-bit data acquisition systems using the SHA 1144, which is compatible with 14-bit ADCs. Sample/hold amplifiers track analog signals until switched to the hold mode, when the signal's value at that time is retained until the 14-bit ADC completes its conversion. Specs are max gain nonlinearity of ±0.001%, max acquisition time of 8 μs, and max gain tempco of 2 ppm/°C. **Analog Devices, Inc,** Rt 1 Industrial Pk, Norwood, MA 02062.

Circle 204 on Inquiry Card

150- AND 300-W TRIPLE OUTPUT SWITCHERS



RS/RT switchers offer two isolated auxiliary outputs in addition to the main 5-V output. The RT153 and -154, packaged in 5 x 5.5 x 9.5″ (13 x 14 x 24.1-cm) T15 cases, output 5 V at 30 A and 5 V at 2 A with the third output 12 V at 5 A for the -153 and 15 V at 4 A for the -154. The -303 outputs 5 V at 60 A, 12 V at 5 A, and 5 V at 5 A. The -304 has the same 5-V outputs as the -303 with the third 15 V at 4 A. Models -303 and -305 are encased in 5 x 8 x 10″ (13 x 20 x 25-cm) T30 packages. **ACDC Electronics, Div of Emerson Electric Co,** 401 Jones Rd, Oceanside, CA 92054.

Circle 205 on Inquiry Card

A Workhorse That's A Winner . . . At 1250 LPM

Model 5321 is an off-the-shelf drum printer, already engineered for your tough jobs. Jobs that demand heavy-duty print cycles, long hours of reliable operation and consistent print quality — at high speed! This is a full-size printer for mainframe-size jobs.

Years of dependable service in countless installations have earned it a reputation as "the workhorse of the computer industry." The MDS 5321 is no slouch. It can produce human-readable or machine-readable hard copy, on a wide 160-column print line, 1-up, 2-up, 3-up or 4-up, at speeds to 1250 lines per minute*.

A variety of type fonts is readily available. Gothic style, IBM-compatible, ECMA, OCR, and CMC 7 or E13B MICR fonts — so important in financial applications where secure check imprinting is involved.

The 5321 is completely buffered. A full line of print data with its associated formatting instructions is stored in memory while the previous line is still being printed. This means maximum throughput and no missed dates for your production schedule — no overruns on your print budget!

*Using standard 48 contiguous characters. 64, 96 and 112 character sets optionally available.

Consider the outstanding features of MDS 5321:

- High-speed paper slewing to 75 ips
- Additional tractor pins to minimize tearing of form holes
- Low-inertia servo motors to considerably reduce maintenance requirements
- Quick-loading VFU mechanism designed for extended form-loop life
- Failure-proof sensing switches for No Paper or Paper Low conditions
- Advanced ribbon mechanism to assure maximum usage of entire spool
- Optional extended interface for additional status monitoring.

The 8-bit interface is already in place. The next move is yours. Whether you're in the OEM business or a systems house specializing in custom applications, it will pay you to look into the MDS 5321. Quantity discounts available. Send coupon today for a detailed Fact Sheet. Or call collect, J. Hill at (315) 866-5300 or J. Engstrom at (714) 772-0803.

MDS MOHAWK DATA SCIENCES

Mohawk Data Sciences — OEM Division
Palisade St., Herkimer, N.Y. 13350
Please send me information on the MDS Model 5321.

Name _____

Title _____

Company _____

Street _____

City _____

State _____ Zip _____

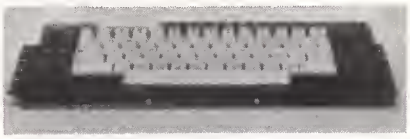
☐ I'm in a hurry. Have a representative call.

CD779

CIRCLE 101 ON INQUIRY CARD

PRODUCTS

CAPACITIVE ENCODED KEYBOARDS



Solid state keyboards, with no mechanical contacts to wear out, use a phase detector in the key scanning system to eliminate electrical noise. N-key rollover and std P/ROM encoding are also included. A rugged 0.0625" (0.159-cm) steel top plate with 90° formed edges eliminates warping, deflection, and the need for extra support. Each keyswitch is rated at 200M operations. Springs are permanently retained to prevent loss. **Amkey, Inc,** 7 Andover St, Andover, MA 01810.
Circle 206 on Inquiry Card

HIGH SPEED FLOATING POINT CONVERTER

Model 5744 transforms floating point binary numbers into 1 of 16 displayed number formats on the Graphic 7 display screen at conversion rates of more than 500/s. Representations include real numbers, scientific notations, latitude and longitude angles, time, and number of days. Additional formats include hexadecimal, octal, binary, and Boolean state by qualifier entry. The converter is bidirectional. **Sanders Associates, Inc, Information Products Div,** Daniel Webster Hwy S, Nashua, NH 03061.
Circle 207 on Inquiry Card

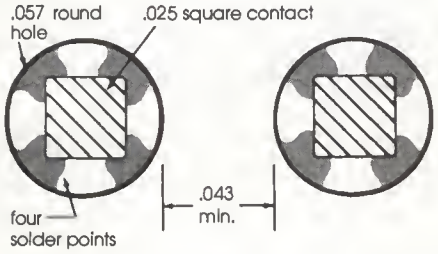
HANDHELD PHOTOGRAPHY SYSTEM FOR VIDEO DISPLAY

By mounting the GDS-1000 camera system, operated by a pistol grip shutter release, on the back of an optical hood customized to each display, an effective "ministudio" is created which correctly aligns the camera to the display, shuts out ambient light, and in the case of Polaroid photography provides an additional sharp focus supplementary lens. Clear black and white or color pictures of all visual displays are reproduced. **GDS Graphic Display System Ltd,** 76 Hemingford Rd, Cambridge CB1 3BZ, England.
Circle 208 on Inquiry Card

No more square tails in round holes.

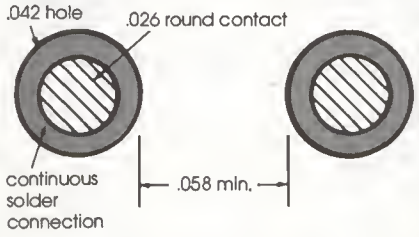
Introducing the wave solder PC connector.

What an electronic design engineer will make-do with in a pinch is astonishing. For example — converting wire wrap* PC connectors to wave solder.



How it's done: you saw off the square .025" tail and push it through a .057" round hole in the PC board. You get only 4 contact points for solder. And there's room for only one tracing between holes. But, so what...it works.

At last — The obvious answer



Our own design engineers, not afraid of doing the obvious and simple thing, have done just that. They've taken a series of our PC wire wrap connectors — and given them .026" round tails. Everything else stays the same: the insulator, semi-bellows contacts, pin and row spacing.

So what?

So — the .026" round pin slips into a .042" round hole in your PC board for an excellent solder connection. So — you can now get multiple tracings between rows.

We have two tail lengths: a .200" short one and a .250" longer one to take the AS400 Solderpak** System. These are available in connectors with contacts on .100", .125" and .156" centers, and in layouts from 6 to 50 positions.

Use our coupon and we'll send you all the details.

There's more. There are some things we haven't told you — including materials and other details you need to know. Ask us for the literature.

NAME _____

TITLE _____ TELEPHONE _____ EXT. _____

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

Viking CONNECTORS

21001 Nordhoff Street, Chatsworth/CA 91311 U.S.A.

(213) 341-4330/TWX: 910-494-2094

*A registered trademark of the Gardner-Denver Company. **A registered trademark of the Raychem Corporation.

CIRCLE 107 ON INQUIRY CARD

PRODUCTS

AUTOMATIC MINI-FLOPPY DISC LOADER

Self-contained 11.5 x 9 x 20" (29.2 x 23 x 51-cm), 25-lb (11-kg) 5"(13-cm) disc loader subsystem sequentially processes up to 50 discs automatically. The 050W-1 stacks up to 50 open or closed flap discs in the input hopper. After completion of a read or write operation, each disc is automatically ejected into the output hopper. Unit may be manually operated. Load and unload cycles require 0.75 s, max. **Media Systems Technology, Inc,** 1616 S Lyon, Santa Ana, CA 92705.
Circle 209 on Inquiry Card

GENERAL PURPOSE MEMORY CARD

Standalone ECOM 137S consists of address registers, data registers, and control circuits necessary for systems interface. Memory capacity is available in 16k-word increments up to 131,072 words. Std word lengths are 18 to 24 bits allowing configurations for systems with parity or ECC. Features include switch selectable address range, TTL interface compatibility, byte control capability, internal or external refresh capability, and battery backup. **Trendata/Standard Memories,** 3400 W Segerstrom Ave, Santa Ana, CA 92704.
Circle 210 on Inquiry Card

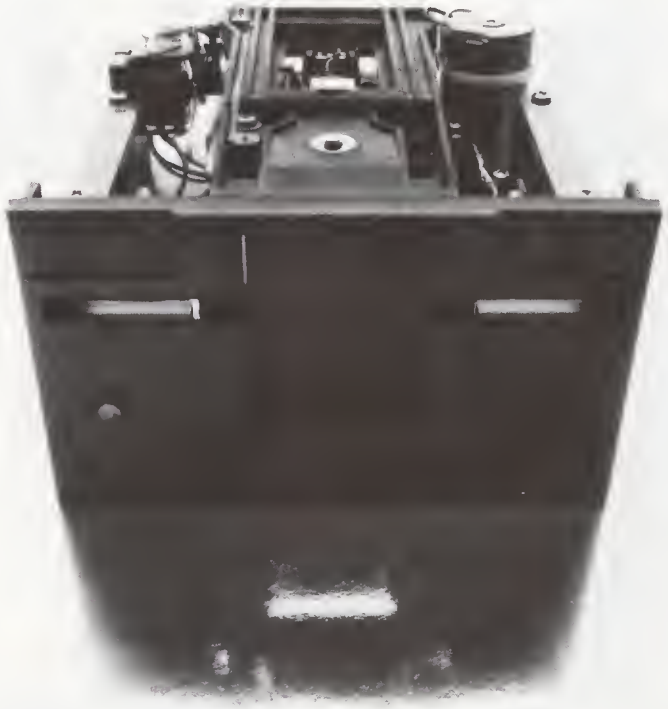
MEDIUM/HIGH SPEED OEM CARD READERS

Model 300, a 400-card/min reader, and model 800, either a 600- or 1000-card/min version, both contain all electronics on a single PCB. The read mechanism is optically based, allowing the series to process mark-sense type cards, 80-col cards, or both. Data inversion is an option on the combination reader; fixed or variable formats are accommodated on the mark sense and combination readers. Hopper and stacker sizes are 500 cards for the 300, and 1000 cards for the 800. **True Data Corp,** 17092 Pullman St, Irvine, CA 92714.
Circle 211 on Inquiry Card

5.5" FLOPPY DISC DRIVE

Single- and dual-head drives all have 40 tracks, an anticrunch feature, and daisy chain capability. A track-to-track access time of 25 ms produces a random avg access time of 340 ms. Model FDD-100-5 for single-density applications accommodates up to 125k bytes; for double density, unformatted storage increases to 250k bytes on each side. Model FDD-200-5 reads and writes data on both sides, storing 500k bytes, without flipping the diskette. **Siemens Corp, OEM Data Products Div,** 1440 Allec St, Anaheim, CA 92805.
Circle 212 on Inquiry Card

The double-headed 5-1/4" floppy with a big difference.



It's available now!

PCC has them. In quantity. Ready for shipment.

Double-headed floppies that are compatible with Shugart down to the last screw hole.

It's the PCC FD-250, the double-headed version of our own FD-200. It can replace the Shugart SA 400 and quadruple your capacity (to as high as 437.5K Bytes).

What the FD-250 means is that right now you can fill up those empty boxes in your systems that are waiting for floppy drives. And you can upgrade from single- to double-sided immediately.

All without re-machining a single screw hole.

For more information on the PCC FD-250—or better yet, to order it in whatever volume you need—call your nearest PCC sales office.

Why wait? Your competition won't.

So. California-(213) 996-1333
No. California-(415) 349-9184
Illinois-(312) 253-2380
Texas-(214) 387-2817
Connecticut-(203) 348-3949
Pennsylvania-(215) 265-8310
New York-(716) 271-2710
Florida-(305) 647-6150
England-(0) 734-582115
Headquarters-(213) 999-2020

PCC PERIPHERALS
PERTEC COMPUTER CORPORATION

PRODUCTS

INTELLIGENT VIDEO DISPLAY TERMINAL

A solid state detachable keyboard, smooth scroll, tilt screen (10 to 15° viewing angle), and large 7 x 9 dot matrix char added to such std features as numeric pad, u/lc char, editing, current loop interface, and cursor addressing enhance the Visual 200 microprocessor based terminal. Switchable emulation capability allows code for code emulation of a Hazeltine 1500,

ADDS 520, Lear Siegler ADM-3A, or DEC VT-52. Self-test diagnostics are provided on power up. **Visual Technology Inc,** Dundee Pk, Andover, MA 01810.
Circle 213 on Inquiry Card

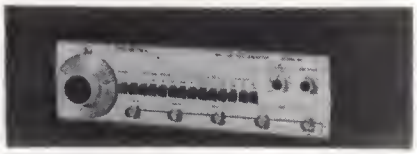
μPROCESSOR DEVELOPMENT LAB EMULATOR PACKAGE

An emulator package for the 8001/8002A Microprocessor Development Labs (MDL) provides complete hardware and software development support for users of the RCA 1802 8-bit CMOS microprocessor. Other capabilities include debugging support, hardware and software integration, and realtime in-circuit emulation of the users' microprocessor based prototype system. The support package includes the 1802 assembler software, emulator, and prototype control probe. **Tektronix,** PO Box 500, Beaverton, OR 97077.
Circle 214 on Inquiry Card

LARGE PRINT COLOR CRT TERMINAL

LPVT is a standalone, RS-232-C compatible, 19″ (48-cm) CRT with 3 user selectable print sizes up to 1.5″ (3.8 cm) high. Eight interchangeable foreground and background colors offer a variety of contrasts. The window feature buffers a screenful of char (80 x 48) from the host, which can be scanned at the user's pace. Keyboard selectable baud rates range from 110 to 9600 (1200 max in large print). Editing functions and separate ASCII keyboard are std. **ARTS Associates, Inc,** 80 Boylston St, Suite 1260, Boston, MA 02116.
Circle 215 on Inquiry Card

2-MHz FUNCTION GENERATOR



A 2-mHz (500 s) to 2-MHz frequency span is covered in 7 overlapping ranges with the model 182. Each multiplier setting gives a full 1000:1 frequency range. Operational modes are continuous, triggered, and gated. High output power drives low impedance and capacitive loads. The high level output is a full 20 V pk-pk from a 50-Ω source, with a max peak current of 100 mA. Both the high and low level outputs may be varied a full 30 dB. **Wavetek,** 9045 Balboa Ave, San Diego, CA 92123.
Circle 216 on Inquiry Card

Mini/Micro79

The Far West Classic in the heart of California Computer Country

Here's a progress report on Mini/Micro79, the far west computer event of the year in the heart of the super-active Southern California computer market-place.

Mini/Micro returns to beautiful Anaheim Convention Center, September 25-27 with a terrific conference program and a timely, sparkling expo of brand-new products from chip-level to full systems, and including a new test instrumentation section.

In the column at the right are the names of 80 fine companies who form the preliminary list of exhibitors. And just below are the titles of 24 solid sessions, as selected by Program Co-chairmen Neil Kelley (Infosystems) and Bob Brown (Hewlett-Packard) and the 1979 Mini/Micro program committee.

The Conference program at a glance

Tuesday

AM
- Pascal on Minis and Micros
- Desktop Computer Applications
- Distributed Processing and Terminal Systems
- Computer Privacy and The Law

PM
- Future Developments in Small Computer Software
- Computer Graphics
- 32-Bit Machines and Other Megaminis
- Maintenance and Fail-Safe Operation

Wednesday

AM
- Military Microcomputers
- Data Base Management Systems for Minis
- Technology Impact on Data Communications
- Mass Memory Storage

PM
- Industrial Microcomputer Applications
- Success with Single-User Computers
- Telecommunications from the Terminal User's Viewpoint
- Printers and Other OEM Peripherals

Thursday

AM
- How Many Bits Do You Need?
- IBM-Software Compatible Minis
- Memories: MOS, Bubbles, and CCDs
- Small Business Computers

PM
- Micro Testing at Chip and Board
- "IBM Watching": Products and Marketing in the Eighties
- Development Software for MPU's
- Establishing Computer Distributorships

An Early-Bird List of Mini/Micro Exhibitors

Able Computer Technology
Addmaster
Aero Mayflower Transit
AFIPS
Anadex Inc.
Avanti
Ball Computer Products
Ball EDD
Benwill Publishing Corp.
Cahners Publishing Co.
Calex Manufacturing
California Computer Products
CAP-CPP Inc.
Centronics
Century Data Systems
Cipher Data Products
Columbia Data
Computer Automation
Computer Business News
Computer Interface Technology
Control Data Corp.
CW Communications Inc.
Data Electronics Inc.
Datum Inc.
Digital Equipment Corp.
Documentation Systems Inc.
Educational Data Systems
EECO
Epic Data
General Automation
Hamilton/Avnet Electronics
Haveg Industries Inc.
Hewlett-Packard, Desktop Computer Division
Hewlett-Packard, Systems Division
Interdyne Company
Intermec
Intel Corporation
International Data Corp.
International Data Sciences
IPI
Jade Computer Company
Kierulff Electronics Inc.
Lear Siegler Inc.
MDB Systems
Megatek Corporation
Memorex
Micom Systems
Microfocus
Mitsubishi Electric
Monolithic Systems Corp.
Moxon Electronics
NCR Corporation
Newport Data Systems
Paradyne Corporation
Printronix Inc.
Racal-Vadic
Randal Data Systems
Ramtek Corporation
Remex
Scientific Micro Systems
Sola Electric
Sord Computer Systems
Space Byte Computer Corp.
Summagraphics
Systems Furniture Company
Tektronix
Tele-Dynamics
Teletype Corporation
Telpar Inc.
Texas Instruments
3M Company
Triple I, Inc.
Western Digital
Western Peripherals
Wilson Laboratories
Wyle/Liberty Electronics

Mini/Micro Computer Conference and Exposition, Robert Rankin, Managing Director

Mini/Micro Computer Conference and Exposition
5528 E. La Palma Avenue, Suite 1A, Anaheim, CA (714) 528-2400

Please send me complete information on Mini/Micro79, to be held Sept 25-27 in Anaheim Convention Center, as follows:

- ☐ Please send me a detailed Preview Program (available August 1) with complete program, registration, and hotel information.
- ☐ Please send me complete information on exhibiting in Mini/Micro79, including floorplan and exhibitor services furnished.

Name _____

Title _____

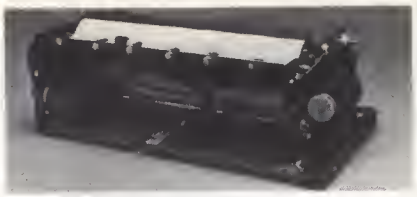
Company _____

Address _____

City, State, Zip _____

PRODUCTS

80-COL, 50-CHAR/S THERMAL PRINT MECHANISM



A microprocessor controlled version of the model Q3 80-col OEM mechanism includes a 45-char buffer for max throughput and generates the full ASCII set of 96 u/lc char in a 5 x 7 dot matrix. The unit features a solid state printhead mounted on a ball bearing carriage, an electronically controlled stepper motor drive, and a patented printhead control mechanism. The printer also includes an efficient paper handling mechanism and adjustable print density. **Computer Devices, Inc,** 25 North Ave, Burlington, MA 01803.
Circle 217 on Inquiry Card

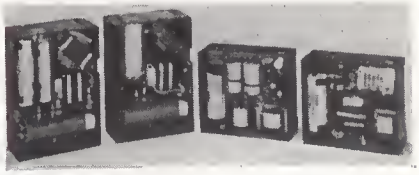
PROGRAMMABLE R-D CONVERTER

High accuracy, programmable resolver to digital converter for industrial control applications features programmable resolution of 12, 13, or 14 bits; tracking rates to 52,000 deg/s, 2600-Hz reference frequency operation; and a worst case accuracy of ±2 arc min ±0.9 LSB. Model 800B104, packaged in a 3.0 x 4.0 x 0.44" (7.7 x 10.2 x 0.12-cm) potted module, will follow accelerations of up to 6200 deg/s² with 1 LSB error. **Control Sciences, Inc,** 8399 Topanga Canyon Blvd, Canoga Park, CA 91304.
Circle 218 on Inquiry Card

12" BLACK/WHITE CRT/KEYBOARD TERMINAL

Preprogrammed single-chip microcomputer and SCT-100 standalone video terminal board combined with 12" (30.5-cm) black and white monitor provide complete video terminal for OEMs and small business systems. Board converts parallel ASCII keyboard input to 1.5-V pk-pk video output. Display is 1024 5 x 8 matrix chars. Features include 128-char set, 56-key keyboard, full cursor control, and direct cursor addressing. Operation is available at 110 to 300 baud ASCII and 45.45/74.2 baud Baudot. **Xitex Corp,** 13628 Neutron Rd, Dallas, TX 75240.
Circle 219 on Inquiry Card

OPEN FRAME SWITCHING POWER SUPPLIES



LY series includes 14 single-output models ranging from 5 to 28 V with currents up to 20 A, and 4 dual-output models available up to ±15 V and 3 A, in 2 package sizes. All models are convection cooled, contain 20-kHz switching circuitry, built-in automatic current limiting, and efficiency ratings up to 70%. Overvoltage protection is available as an accessory. Line regulation is 0.1% for all models; tempco is 0.03%/°C. **Lambda Electronics, div of Veeco Instruments Inc,** 515 Broad Hollow Rd, Melville, NY 11747.
Circle 220 on Inquiry Card

Memorex OEM: Come and get it!

That's our way of saying the Memorex® 601 Winchester-type disc drive is available. Right now. In 25, 50 or 75 megabytes. With fixed head operation.

Memorex has been in the OEM business for over 12 years. We've been in full production on our Winchester-type drive since 1976. Behind every 601 is an investment of over $25,000,000 and 90,000,000 hours in Winchester technology. And the 601 is available for immediate delivery. In quantity. To order your 601 evaluation unit today, give us a call:

Northern California	Carl Burke	(408) 987-1373
Southern California	Jim Felt	(714) 891-2541
Boston, Massachusetts	Mike Weinstein	(617) 890-0700
	Jack Losh	(617) 890-0700
Dallas, Texas	Gary Beebower	(214) 258-3510
Denver, Colorado	Jack Helman	(303) 837-0205
Detroit, Michigan	Bob Baughman	(313) 354-4511
West Orange, New Jersey	Ed Gittines	(201) 325-0164

MEMOREX
DISC DRIVE DIVISION
We deliver product not promises.

Memorex products include data storage subsystems, telecommunications equipment, computer media, and audio and video tape.

CIRCLE 112 ON INQUIRY CARD

PRODUCTS

CERTIFIER FOR PICCOLO 8" DISC

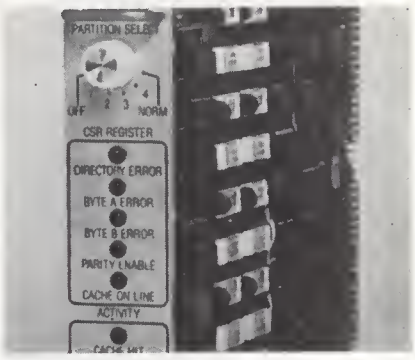
Model 3PX358 is a self-contained, internally programmed single-disc certification system with microprocessor controlled automatic and manual test capability for IBM's Piccolo mag disc. A 16k RAM provides program and test data storage. A remote CRT

terminal console and keyboard serves as the operator control center. Hard-copy printers are available for a permanent record of disc test results. **Three Phoenix Co,** 21639 N 14th Ave, Phoenix, AZ 85027.
Circle 221 on Inquiry Card

GPIB PROGRAMMABLE NETWORK ANALYZER

Swept measurements of transmission loss or gain, return loss (SWR), and absolute power, from 10 MHz to 34 GHz, are provided by model 560 scalar network analyzer. Any two measurements may be displayed simultaneously. Dynamic range is 16 to −50 dBm, with 40-dB directivity. Continuously variable controls enable precise positioning of display traces. LED readout at any trace point displays values with 0.1-dB resolution. With GPIB remote control, data are digitized to 0.01-dB resolution. **Wiltron Co,** 825 E Middlefield Rd, Mountain View, CA 94043.
Circle 222 on Inquiry Card

PLUGGABLE CACHE MEMORY



Series 8000 provides plug compatible cache memory for DEC's PDP-11/34, /35, and /40. The cache has 4k x 25 memory that can store 8k bytes of data. Address map partition maximizes system enhancement by adding memory flexibility. A parity error circuit with LED indicators is incorporated and a Unibus addressable CSR allows cache to be turned on and off from the front panel. Diagnostic software is included. **Minntronics Co, Inc,** 2599 White Bear Ave, St Paul, MN 55109.
Circle 223 on Inquiry Card

REPORT PROGRAM GENERATOR PACKAGE

RPG II creates, retrieves, updates data files, and simplifies the designing and processing of reports. Compatible with System/3 RPG II, the package features sequential, indexed sequential, and direct access to data files, special input functions, lookahead fields, bit setting, and/or operators, automatic field numbering, and COBOL compatible subroutine calls. Virtual memory operating system (VULCAN) extends availability by permitting multiple users to prepare reports while other processing functions are being performed. **Harris Corp, Computer Systems Div,** 2101 W Cypress Creek Rd, Fort Lauderdale, FL 33309.
Circle 224 on Inquiry Card

IT'S NO WONDER EVERYONE'S TRYING TO MATCH OUR TRACK RECORD.

After all, it's pretty impressive.

With over 20,000 units shipped, we're already Number 2 in the marketplace.

That's because our MegaFlappy™ disk drives give you all the capacity of an 8-inch floppy in a 5¼-inch format. Ordinary 5¼-inch floppies provide just 35 tracks/drive, and store only 70K bytes. Not nearly enough to be efficient. But our MegaFloppy disk drive uses 77 tracks to yield a capacity of up to 946K bytes per drive.

That's more than ten times an ordinary 5¼-inch floppy.

But there are other reasons everyone's trying to catch us. Dozens of competent OEMs are committed to our approach, and are currently offering products featuring our MegaFloppy drives. And other large OEMs are coming over to our side and delivering to their customers all the advantages of our remarkable 5¼-inch drives.

The MegaFlappy disk drives came equipped with a stainless steel lead screw, coupled with a metal follower. Which provides more precise positioning than plastic cams or plastic followers – and with greater reliability.

And our media protection is practically foolproof. Interlock protection and tactile feedback when diskette is inserted help prevent damage to your media. Media that you can't afford to lose.

MICROPOLIS™

Where the 5¼-inch drive grew up.

This same technology goes into every one of our MegaFlappy disk drives. Whether they're double density single drives with single or dual heads. Or dual drive models featuring the Micropolis Intelligent Controller.

So if you're interested in a flappy that'll make you forget the one you're using now, think about our MegaFlappy disk drives.

Most other flappy drive manufacturers already are.

For a descriptive brochure, in the U.S. call or write Micropolis Corporation, 7959 Deering Avenue, Canoga Park, California 91304. Phone (213) 703-1121. Or, better yet, see your local representative.

CIRCLE 114 ON INQUIRY CARD

PRODUCTS

103/113B COMPATIBLE MODEM

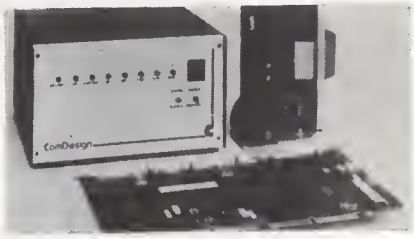
Answer-only 300-bit/s direct connect model DL 113B is FCC registered and requires no DAA. A 7" (18-cm) package houses up to 16 modems, plus a master test module with 8 LED indicators to display status of selected modems. Modules may be replaced from the front without disturbing EIA

or telephone line connections. Failure of an individual module will automatically cause that line to go busy and will not affect other lines. **Infotron Systems Corp,** Cherry Hill Industrial Ctr, Cherry Hill, NJ 08003.
Circle 225 on Inquiry Card

NATIVE PASCAL LANGUAGE FOR VAX-11/780

Developed with the U of Washington, Seattle, the reentrant, native mode PASCAL compiler uses the hardware floating point and char instruction sets and the virtual memory capability of the VAX/VMS operating system. Extensions include sequential files of fixed or variable length records, a double precision real data type, and a value declaration part. Separate compilation of modules and a call interface to programs written in other native VAX/VMS programming languages are std. **Digital Equipment Corp,** Maynard, MA 01754.
Circle 226 on Inquiry Card

TERMINAL CONCENTRATOR



TC-3 Concentrator combines the functions of an 8-line Unibus asynchronous interface and add-on statistical multiplexer, allowing PDP-11, DECsystem-2020, and VAX users to add remote terminals and printers. Features include error correction, data compression, and online terminal diagnostics. Local unit has functional characteristics of a DZ11-A interface; standalone remote concentrator communicates with local unit by direct wire connection or full-duplex 1200- to 9600-baud leased line. **ComDesign, Inc,** 340 S Kellogg Ave, Suite A, Goleta, CA 93017.
Circle 227 on Inquiry Card

STANDALONE PUNCHED PAPER TAPE INTERFACES

The RJR2321 single-port interface for punched paper tape readers, the RJA2321 single-port reader/perforators, and the RJA2322 dual-port interface for combos adapt any of the company's related devices to communications roles. Single-port models are connected to a data communications model or directly to the host computer. The dual-port model includes the model port and a separate current loop interface for connecting the reader/perforator to a CRT terminal, teletypewriter, or printer. **Remex Div of Ex-Cell-O Corp,** 1733 Alton St, Irvine, CA 92713.
Circle 228 on Inquiry Card

What does our new super-fast, super-silent Model 3901 Band Line Printer have in common with all other DPC Band Line Printers?

About 95%.

While maintaining greater than 95% parts commonality, DPC's Band Line Printers are now available in two separate series: The original pedestal-mounted Series 3000 (4 models offering line speeds from 75-600 LPM) and the new fully-enclosed, super-silent Series 3001 featuring 4 models ranging from 150-900 LPM with standard character sets.

Specifically, the Model 3901, an 1100 LPM printer on 48 characters, has the horse-power and the staying power to be a mainstay in your main computer room—or serve as a quick, quiet remote terminal.

More details on request, and your requests are sincerely welcomed.

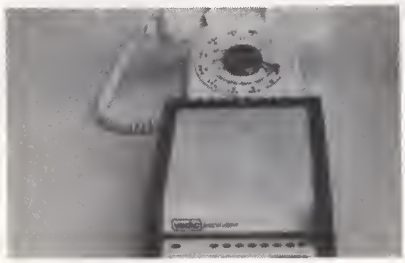
DATA PRINTER CORP
99 Middlesex Street, Malden, MA 02148
Tel: (617) 321-2400 TWX: 710-348-0794
Regional Sales Offices: Clifton, NJ, Santa Ana, CA

Model 3901
1100 LPM/48 Characters

CIRCLE 116 ON INQUIRY CARD

PRODUCTS

1200-BIT/S HALF-DUPLEX MODEM



VA1250/55 series modems for remote terminal users plug directly into the std telephone voice jack (RJ-11C) or data jacks (RJ-41S or RJ-455). Models are also available for leased line applications. As direct replacements for Bell 202C, 202E, and 202S modems, the series offers switchable options, such as line current disconnect for unattended operation. Problems in the network are isolated using an interface display, coupled with the local loopback, and force request to send (RTS). **Racal-Vadic,** 222 Caspian Dr, Sunnyvale, CA 94086.
Circle 229 on Inquiry Card

RAMIS SYSTEM FOR MINICOMPUTER

Suited to distributed processing systems, RAMIS 3200, a RAMIS II system designed for optimum performance in the NCSS 3200 environment, provides all previous version capabilities in a flexible user oriented, IBM compatible package. It integrates an English like, nonprocedural language for report preparation and records management into a comprehensive database management system. **Mathematica Products Group, a div of Mathematica, Inc,** 14 Washington Rd, Princeton, NJ 08540.
Circle 230 on Inquiry Card

EXTRUDED JACKET CABLING

Computer and electronic systems requiring cabinet to cabinet interconnections will benefit from the Spectra-Guard™ line that encompasses all of the company's cables. An extrusion process encapsulates conductors (up to 64) inside an extruded (60-mil) outer jacket. It is available with or without integral emi/rfi shielding and 2 drain wires. The process gives low crosstalk, consistent electrical characteristics, and high flexibility. **Spectra-Strip div of Eltra Corp,** 7100 Lampson Ave, Garden Grove, CA 92642.
Circle 231 on Inquiry Card

CARTRIDGE TAPE DRIVE WITH RS-232 INTERFACE

Microprocessor based tape drive with RS-232 interface uses an ANSI/ECMA 0.25" (6.35-mm) cartridge. Commercial, ruggedized, and Mil spec versions are available with or without power supply, with emi front panel, or in full emi enclosure. Commercial units are furnished with either front or top cartridge loading. Data rates are selectable from 110 baud to 19.2k baud. Self test and tape positioning algorithm upon power-on insure proper operation. **Data Electronics, Inc,** 370 N Halstead St, Pasadena, CA 91107.
Circle 232 on Inquiry Card

HIGH MEGOHM DIP RESISTOR NETWORK

Made up of individual thick film chip resistors, each encapsulated with a protective epoxy coating, resistor network is useful in telecommunication circuitry. Advantages of using components packaged in DIP housings include easy handling and correct assembly of critical components. Resistance values range from 1×10^6 to 2×10^{11} Ω. TCR is −0.1%/°C, operating voltage is 60 V, and operating temperature is −50 to 150 °C. **Eltec Instruments, Inc,** PO Box 9610, Daytona Beach, FL 32020.
Circle 233 on Inquiry Card

DATA COMMUNICATIONS TEST INSTRUMENT

The monitoring and diagnostic instrument provides 3-level programming: the first level provides "canned" programs, the second allows operation in DICOL mode, and the third permits more complex programs using a modified language, COMBASIC. Inherent features of Encore 100 are a full ASCII keyboard, operator prompts displayed on the CRT, and a 9" (23-cm) CRT display. A subscript feature points out errored char, block check, and frame check data. **Digitech Data Industries, Inc,** 66 Grove St, Ridgefield, CT 06877.
Circle 234 on Inquiry Card

A lot of complex thinking goes into the Teletype* model 40 printer. And, incredibly, it all fits on this 9″ by 19″ circuit card.

More brains; less brawn.

That's the advantage of an electronic printer like our 300 LPM model 40 series. The LSI (Large Scale Integration) circuitry tucked underneath the printer can perform functions with greater reliability than mechanical hardware.

And it can perform them in a fraction of the time with a fraction of the parts. Plus, fewer moving parts means less maintenance and increased printer life.

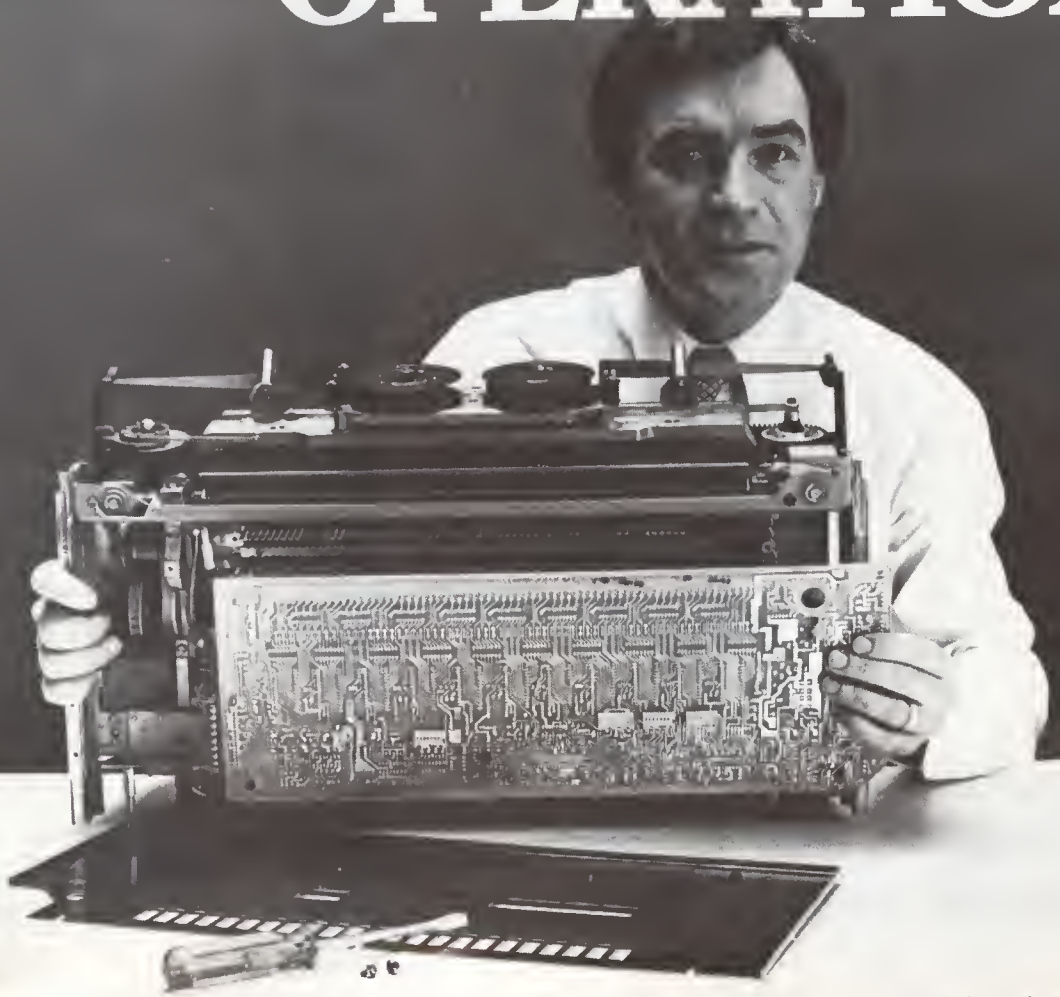
All you have to do is plug it in.

Just attach the AC power and a serial signal source and your model 40 is ready to go to work. There are 32 switch-selectable options and self-diagnostics available at no additional cost. Housed in an attractive cabinet, if you need one. And our technical assistance is never extra.

So for not much money, the brains behind our operation can become the brains behind yours.

Teletype Corporation
5555 Touhy Avenue, Dept. 3185, Skokie, IL 60076.
Telephone (312) 982-2000.

MEET THE BRAINS BEHIND THE OPERATION.

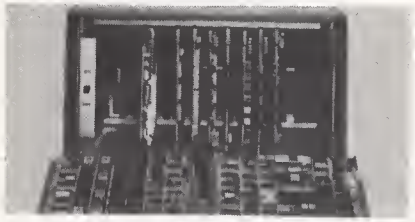


*Teletype is a trademark and service mark of the Teletype Corporation

CIRCLE 118 ON INQUIRY CARD

PRODUCTS

ATE DATA COUPLER FOR BASIC LANGUAGE PROGRAMS



Microprocessor based 53A-MPX can be used to create standalone data acquisition and control system or can function as intelligent satellite in distributed processing system. As satellite, it can be either hardwired or connected via modems with up to 16 satellites on a single multidrop circuit. Unit incorporates communication executive that allows central CPU to download and run BASIC language programs in remote satellites. I/O buffers store data so that neither CPU nor system delay each other. **Computer Data Systems, Inc,** 186-58 Homestead, Morrison, CO 80465.
Circle 235 on Inquiry Card

FIREPROOF RESISTORS FOR SURGE APPLICATIONS

Fireproof semiprecision resistors for pulse loading and surge discharge applications, PPW series devices are made of alloy wire wound on a ceramic core. The element is sealed in a ceramic case with fireproof, inorganic material, and all internal connections are welded. Six power ratings are available from 2 to 15 W. Resistances range from 1 to 1600 Ω for 2-, 3-, and 5-W sizes, to 1 to 2500 Ω for 7-W size; and from 1 to 5000 Ω for 10- and 15-W sizes. **TRW/IRC Resistors,** PO Box 1860, Boone, NC 28607.
Circle 236 on Inquiry Card

OPTICAL ABSOLUTE POSITION ENCODER

5VL80 series shaft position encoder uses a single LED light source, as opposed to multiple sources, to maintain reliable operation over the op temp range. Other features include resolution of up to 2^{10} bits/turn, single 5-Vdc operation, nonambiguous codes, and TTL compatible outputs. The unit is housed in a size 25 package. **Digital Products Div, BEI Electronics, Inc,** 1101 McAlmont St, Little Rock, AR 72203.
Circle 237 on Inquiry Card

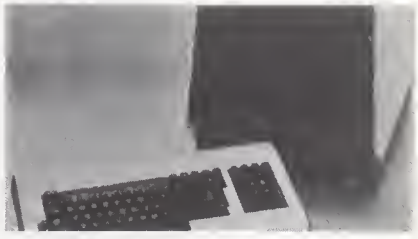
MECHANICAL INDICATOR ROCKER SWITCHES

Mechanically displayed legends on Rockette switches indicate switch function. A color coded strip or legend appears through windows in rocker button, giving positive indication of switch position without need for illumination, indicator lights, or hot stamped legends. Units are available with serrated or smooth rockers; 1 or 2 windows; in red, white, or black; subpanel; flush or snap-in mounting; and 1- or 2-pole circuits at ratings from 6 to 20 A at 125 Vac. **Cutler-Hammer, Commercial Controls Div,** 4201 N 27 St, Milwaukee, WI 53216.
Circle 238 on Inquiry Card

GPIB CONTROLLER

Providing talker, listener, and controller capabilities for the GPIB bus, 7488/18 GPIB controller links the STD microprocessor bus to more than 300 different IEEE bus compatible instruments to configure microprocessor controlled ATE systems. Linked with a DMA module, it can send or receive data at rates to 250k bytes/s. It may also be used in an interrupt driven or polled mode of operation. **Ziatech Corp,** 2410 Broad St, San Luis Obispo, CA 93401.
Circle 239 on Inquiry Card

VT-100 COMPATIBLE CRT TERMINAL



DT80/1 interfaces with a printer in 3 modes: online as data comes in, as a printer controller, and as a source for feeding data from the screen directly to the printer. The aluminum housed unit contains a built-in CRT saver and self-diagnostics. The CRT screen holds 24 lines x 80 or 132 char; the user may employ a split screen, double-high or double-wide char, composite video I/O, and limited graphics. The terminal houses an LSI CRT controller with 2 serial I/O ports. **Datamedia Corp,** 7300 N Crescent Blvd, Pennsauken, NJ 08110.
Circle 240 on Inquiry Card

Micro Power

Microcomputer with printer–$375. That's Rockwell Micropower.

For learning, designing, work or just fun, Rockwell's AIM 65 microcomputer gives you an easy, inexpensive head start.

- 20-Column Printer and Display
- Dual Cassette, TTY and General-Purpose I/Os
- R6502 NMOS Microprocessor
- System Expansion Bus
- Read/Write RAM Memory
- PROM/ROM Expansion Sockets
- Advanced Interactive Monitor Firmware
- Big Terminal-Style Keyboard

For more on AIM-65 and how you can develop programs in assembly language or BASIC, write Microelectronic Devices, Rockwell International, D-727-A4, P.O. Box 17479, Irvine, CA 92713 or phone (714) 632-3729, or contact your local Hamilton-Avnet office.

Rockwell International

...where science gets down to business

CIRCLE 120 ON INQUIRY CARD

PRODUCTS

DUAL-TRACK CARTRIDGE DRIVE

DCD-2 data cartridge drive operates at density of 3200 fr/in (1259/cm) on 2 tracks and permits a capacity of up to 672k 8-bit bytes (using PE recording, unformatted) on std DC100A data cartridges. Wide track design ensures high reliability. Low error rate is enhanced by 0.068" (1.727-mm) write and 0.058" (1.473-mm) read track width. Completely bidirectional drive operates at 30 in (76.2 cm)/s for reading and writing functions; search function may be commanded to execute at 30 or 60 in (76.2 or 152.5 cm)/s. **3M Co, Mincom Products Div,** PO Box 33600, St Paul, MN 55133.
Circle 241 on Inquiry Card

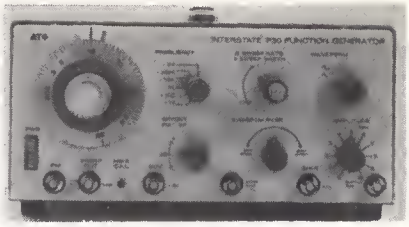
DUAL-SPEED MODEM

An FCC certified 2-wire full-duplex dial line modem, the 300/1200 provides Bell 212A compatibility at 1200 bits/s through PSK modulated synchronous or char asynchronous operation. It also allows Bell 100 series compatibility at rates up to 300 bits/s through FSK modulated asynchronous operation. Integral diagnostics are std; 16 options, including automatic answer, are available. The unit works as 2 modems to provide originate/answer transmission and reception of serial binary data. **Penril Corp,** 5520 Randolph Rd, Rockville, MD 20852.
Circle 242 on Inquiry Card

AXIAL FANS WITH LUBRICANT RETENTION

Patented Recirk™ lubricant retention system used in Brute series fans can double their life. For power supply applications, units are available with built-in transformer. Packages operate at 50 or 60 Hz from 115 to 220 V and are available in either intake or exhaust designs, with or without venturi and optional finger guards. With optional low voltage multioutput transformer, TransBrute® configuration, package offers several voltages. **Gould, Inc, Electric Motor Div,** 1831 Chestnut St, St Louis, MO 63166.
Circle 243 on Inquiry Card

3-MHz SWEEP/FUNCTION GENERATOR



Model F-30 provides low distortion sine, square, and triangle waveforms in the 0.03-Hz to 3-MHz frequency range at levels up to 10 V pk-pk into a 50-Ω load. As a sweep generator, the unit has a linear sweep up to 1000:1 with sweep time variable from 30 ms to 20 s. Other specs include accuracy of ±2% of full scale, 0 to 50 °C operating temperature, and 115-Vac ±10% or 230-Vac ±10% at 50 to 4000 Hz, 25-W max power requirements. **Interstate Electronics Corp,** 1001 E Ball Rd, Anaheim, CA 92803.
Circle 244 on Inquiry Card

PERMANENT MAGNET MOTORS

M5000 line of NEMA 56 frame permanent magnet dc motors rated from 0.125 to 1 hp is designed for rugged use in industrial applications. Units operate at Class B temps, use high capacity bearings, and have constant force brush springs. Line has also been designed for voltages ranging from 12 to 115 Vdc, with versions available for either SCR or pure dc power sources. **RAE Corp,** 5801 W Elm St, McHenry, IL 60050.
Circle 245 on Inquiry Card

DIGITAL PULSER PROBE

DP-100 generates a single pulse in one-shot mode or a 5-Hz pulse train in continuous output mode. It can be used alone, or in conjunction with a logic probe or oscilloscope. When probe output is applied to circuit, it automatically pulls existing logic low to high state or existing high state to low. Observing change in circuit output allows user to isolate faulty circuits and components. Applied test energy is limited to 0.33% of normal power dissipation of a good device. Unit is compatible with DTL, TTL, RTL, and CMOS circuits. **B&K-Precision, Dynascan Corp,** 6460 W Cortland St, Chicago, IL 60635.
Circle 246 on Inquiry Card

Technology *plus* Marketing *equals* Information Transfer

The equation tells it all about Wescon, the West's largest high-technology electronics exhibition and convention. Three days of person-to-person contact and hands-on demonstrations of new products and systems, together with examination of the leading-edge technology that will influence electronics in the decade of the 1980's.

Want to walk into Wescon/79 in San Francisco, sweep by the registration lines, and proceed directly to the exhibit floor or Professional Session? It's easy. Just fill out the registration form below and mail it to us before August 31, together with your check for $3. We'll do the rest — before Wescon opens September 18, you'll receive an embossed admission badge, by mail, entitling you to speedy entrance into Wescon.

One more thing: the pre-registration price is only $3. That's a $2 savings over what admission will cost you at the door.

Clip and mail the registration form today, to:
Wescon/79, 999 North Sepulveda Boulevard, El Segundo, California 90245.

Clip and Mail Today

Wescon 79

PERSONS UNDER 18 YEARS OF AGE NOT ADMITTED

Please PRINT as you want shown on badge.

Name

FIRST OR INITIALS LAST

Position

Telephone (OPTIONAL)

AREA CODE NUMBER

Company/Organization

Address: Bus. or Home

City, State, Zip Code

STATE ZIP CODE

CIRCLE ONE LETTER IN EACH BLOCK

YOUR POSITION	A	Corporate/technical management
	B	Design/specifying engineer
	C	Engineering/manufacturing technician
	D	Engineering services
	E	Sales/Marketing
	F	Purchasing/Procurement
	G	Educator/Student
AREA OF MAIN PRODUCT INTEREST	H	Active components
	I	Passive components
	J	Hardware
	K	Tools & production equipment
	L	Computers
	M	Computer peripherals
	N	Control systems & components
	O	Electro-optical components
	P	Enclosures
	Q	Instruments, indicating
	R	Instruments, control
	S	Mechanical components
	T	Microwave components & systems
	U	Power sources
	V	Wire, cable & connectors

September 18-20, 1979
Civic Auditorium/Brooks Hall
San Francisco

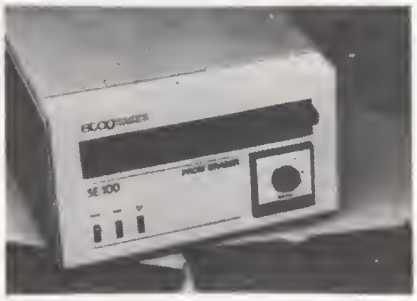
Sponsored by San Francisco Bay Area and Los Angeles Councils of IEEE, and the Northern and Southern California Chapters of ERA.

PRODUCTS

COMPUTER TO SYNCHRONOUS DEVICE INTERFACE

A microprocessor based unit that interfaces up to 30 asynchronous devices with computers supporting IBM 3271 terminal controllers is available with up to 32k of buffer memory. CA12-SIU/3271 is a protocol conversion processor that ties into the same multidrop lines as actual 3271 controllers or the same processors to expand operations. It supports line speeds from 50 to 9600 baud. Front panel indicators include memory overflow, restart, and an active/error pair for each port. **Industrial Computer Controls, Inc,** 196 Broadway, Cambridge, MA 02139.
Circle 247 on Inquiry Card

EPROM ERASER



Bulk erasing EPROMs or single-chip programmable microprocessors, SE100 emits high intensity short-wave ultraviolet radiation. It can erase 104 EPROMs simultaneously or accommodate a complete circuit card. Safety features disable the UV source when the drawer is removed; the timer switches off the lamp after the prescribed UV dosage. The lightproof device has indicators on the front panel to show power-on, erase, and lamp fail. **Stag Systems,** 2465 E Bayshore Rd, Suite 329, Palo Alto, CA 94303.
Circle 248 on Inquiry Card

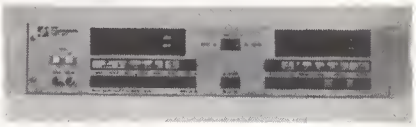
300-W SINGLE-OUTPUT SWITCHERS

Six open and closed frame convection cooled models comprise the S300 series, with voltage ratings of 5 to 28 V and current ratings from 10.7 to 60 A. Line and load regulation is 0.1%, ripple and noise is 50 mV pk-pk, and nom efficiency is 75%. All units have a wide range dual ac input, 20-ms min hold up for loss of line, emi suppression, and overvoltage protection. Other features include input surge current limiting and protection against input voltage transients. **Deltron Inc,** Wissahickon Ave, North Wales, PA 19454.
Circle 249 on Inquiry Card

1200-BIT/S BELL COMPATIBLE MODEM

Connecting directly to the public switched telephone network without the need for leasing a Bell System DAA, the 7202S provides either automatic or manual answering and operates half-duplex on 2-wire lines. The 0- to 1200-bit/s device has self-test and loopback test capabilities. Two switches select test modes, and 9 indicator lamps display control and data functions to simplify fault analysis. The modem is Bell 202S (or CCITT V.23) compatible. **Tele-Dynamics Div, AMBAC Industries, Inc,** 525 Virginia Dr, Fort Washington, PA 19034.
Circle 250 on Inquiry Card

CENTRAL OFFICE TRANSMISSION TEST SYSTEM



Model 1701 transmission test system (TTS) combines level, noise, and frequency measurements with a variable frequency oscillator. It operates standalone or as part of integrated testboard. Two digital displays simultaneously indicate level and frequency of signal being measured or tone being sent. Rapid adjustment of test tone level and frequency is enabled by 2-way individual digit control switches together with digital display panels. Pushbutton indicator switches select proper send or measure line matching impedances. **ADC Telecommunications,** 4900 W 78th St, Minneapolis, MN 55435.
Circle 251 on Inquiry Card

NOTHING TO FORGET. NOTHING TO REGRET.

INTRODUCING THE DATAMEDIA DT80/3 TERMINAL

Until now, picking a terminal you could live with hasn't been easy. Mostly because you had to peer into the future to decide which of a long list of options would eventually be useful. And run the considerable risk of missing one or two that you would later regret not having.

That's why we built the new DT80/3, an advanced terminal with all of the options built right in.

The DT80/3 is the latest member of Datamedia's all-new Series 80 line of CRT terminals. Like all Series 80 terminals, it offers superior performance plus the peace of mind of a full one-year warranty. And the DT80/3, in particular, offers a multitude of special features which will be as valuable in the future as they are today.

For starters, you get a complete video package with features like multi-page display, buffered operations, composite video output, advanced editing functions, and a 128-character ASCII display set. All standard. Plus a 25th display line for special error and status messages, and a special CRT Saver feature which automatically turns off the display after periods of inactivity.

The DT80/3 also gives you the space flexibility of a detachable keyboard, and the ability to set typewriter style tabs for tabbing both forward and back, even in format mode.

An excellent communicator, the DT80/3 speeds data at up to 19,200 baud, synchronously or asynchronously, and offers printer sharing, daisy chaining and/or an auxiliary serial interface. An industry-compatible parallel port also allows for higher speed data transfers for mass storage devices or line printers. And should the DT80/3 ever run into a problem, it will communicate with you, too, through a built-in audible alarm and a series of self-diagnostics.

Best of all, Datamedia's DT80/3 fits comfortably anywhere, measuring a very compact 14" x 14" x 14", and weighing just 37 pounds.

Look at it this way: You can either worry about adding features. Or you can get all the features, right from the start, in the DT80/3.

That's the one option we think you'll be happy to choose for yourself.

Please send me more information on the DT80/3.

Name_____ Title_____

Company_____

Address_____

City_____ State_____ Zip_____

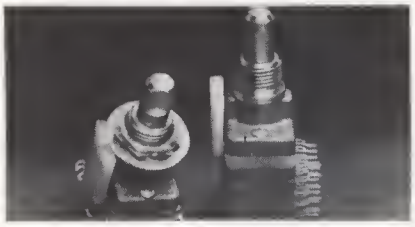
Phone_____

Datamedia Corporation

7300 N. Crescent Blvd., Pennsauken, N.J. 08110
Tel: (609) 665-2382 TWX: 710-892-1693

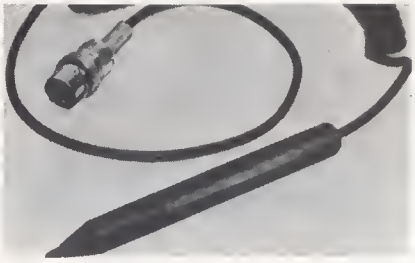
CIRCLE 123 ON INQUIRY CARD

SUBMINIATURE ROTARY SWITCH WITH 0.25" SHAFT



Series 80 switches with optional 0.25" (0.635-cm) dia shaft and 0.375" (0.952-cm) dia bushing complement the std line. The larger diameter bushing is available in lengths up to 0.375" (0.952 cm) with 0.25" (0.635 cm) std. All devices are fully enclosed and environment proof. They are modular, feature a rectangular 0.8125 x 0.5625" (2.063 x 1.429-cm) switch body, and can be used for either PCB insertion or solder lug applications. **Stackpole Components Co,** PO Box 14466, Raleigh, NC 27620.
Circle 252 on Inquiry Card

LIGHTPEN



High performance model LTP-105 features high emi immunity and high scan rate response. A slim body dimension—0.625" (1.59 cm) OD and 6" (15 cm) long—with tapered narrow head permits easy aiming on the target surface. A single 5-V power supply is required. Max scan rate responses up to 5000 cm/ms are typical. Elimination of mechanical switching in the circuit increases performance life. **Photobell Co,** 162 5th Ave, New York, NY 10010.
Circle 253 on Inquiry Card

19" COLOR DISPLAY CRT

Specifically designed for alphanumeric data display, 19VCD1000 is capable of displaying text, data, or graphic information in small, easy to read characters with sharpness and clarity comparable to monochrome tubes. Three primary colors plus additive color combinations are available for color coding, highlighting, or enhancing. Tube is equipped with Chromatrix dark surround negative guard band screen and fine resolution tri-dot rare earth phosphor system. **General Telephone & Electronics Corp, Electronic Tube Div,** 700 N Pratt St, Ottawa, OH 48576.
Circle 254 on Inquiry Card

DATA BASE MANAGEMENT SYSTEM ENHANCEMENTS

Recent release of System 2000® DBMS is said to improve CPU performance of IBM compatible, CDC, and Univac systems up to 59%. Performance is affected in both PLEX (system's extension to COBOL, FORTRAN, PL/1, and Assembler languages), and self-contained language environments. Enhanced areas include high volume multiuser processing applications, in capability to interface virtually any proprietary software package via universal software interface (USI), and in query/update languages through query/update extension (QUEST) have been noted. **MRI Systems Corp,** 12675 Research Blvd, Austin, TX 78766.
Circle 255 on Inquiry Card

RACKMOUNTED ALPHANUMERIC PRINTER

For use in ATE applications, the SP-310 5 x 7 dot matrix impact printer provides 40-col printing at 50 char/s. Microprocessor control allows special functions such as tab and double-width printing. RS-232 and 20-mA inputs are std. Baud rate is 110 to 9600, adjustable. The unit prints on std 3.875" (9.8-cm) paper. A triple line input buffer is optional. Also featured are selectable parity and stop bits, and multiple copy capability. **Syntest Corp,** 169 Millham St, Marlboro, MA 01752.
Circle 256 on Inquiry Card

NO SYSTEM DIAGNOSES LSI FASTER THAN THIS SYSTEM.

No doubt about it.

In board testing, you have to have fast diagnosis before you can have high throughput. And Teradyne's L135 LSI Board Test System delivers the fastest diagnosis in the industry.

What's more, the L135 is the only practical means for production testing LSI. Because only the L135 is engineered to handle the long bidirectional buses and multi-pin devices that stop other test systems cold.

THE ELECTRONIC KNIFE CUTS THROUGH TO BAD DEVICES.

Regular guided probing can only take you so far. Specifically, to the failing bus or node.

That's where Teradyne's Electronic Knife takes over. With a few additional probes, the Electronic Knife precisely identifies the faulty IC.

Costly trial and error replacement of LSI chips is eliminated. Skilled technicians need not spend hours searching out problems.

The L135 even handles multi-layer boards and low-power driver families. Finding faults that can only be detected with the board powered and active.

So the Knife cuts two ways. It cuts diagnosis time for higher throughput, and it cuts operating costs for higher profitability.

PROBES ARE FEWER AND FASTER.

LSI chips are simply too complex for regular probing. Back-tracing the failing signal path may require hundreds of successive, time-consuming probes.

To solve this problem, Teradyne developed a software routine called State Sensitive Trace. It analyzes the circuit and directs the probe first to those inputs most likely to contain the failing signal.

Total probes are reduced from hundreds to, say, 20 or 30.

Also, the L135's On-Line Circuit Model cuts probing time still further. By displaying successive probe commands without the delays other systems may require.

If you're testing conventional boards, the L135 will give you the fastest diagnosis available. If your boards are LSI, only the L135 has the capability to test them on the production line.

Remember that. Because productivity is the bottom line.

For more information on these and other L135 features, contact your local Teradyne Sales Office. Or call Teradyne Boston, (617) 482-2700.

PRODUCTIVITY IS THE BOTTOM LINE.

TERADYNE

CIRCLE 125 ON INQUIRY CARD

PRODUCTS

DATA COMMUNICATION NETWORK ENCRYPTION DEVICE

Electronic devices designed to prevent unauthorized access to computer information transmitted over data communication networks, Datacryptor units operate according to the Data Encryption Standard (DES) algorithm as approved by the National Bureau of Standards. Designed for synchronous, binary synchronous, and SDLC applications, the device enciphers and deciphers up to 9600 bits/s of main channel data in point to point, multipoint, or multidrop networks, providing a high degree of data security for users that include banks, insurance firms, commodities organizations, and other users of computer information. **Racal-Milgo, Inc,** 8600 NW 41st St, Miami, FL 33166.

Circle 257 on Inquiry Card

20M-BIT/S DATA TRANSMISSION TEST SET

Model 604M is used to test, evaluate, and maintain data transmission equipment and systems operating in the range of 10 through 20M bits/s. The unit monitors and displays bit errors, bit error rates, number of errors/block, number of errors/second, and test duration in terms of either total number of blocks or total number of seconds. Self-diagnostic capability includes clock and data loopback, insert error, and slip sync. Outputs are provided for external counters and recorders and a parallel BCD 10-col printer interface for direct bit error rate and alarm printout. Operational features include full- or half-duplex, or simplex operation, selectable block size/test period, error block/error second thresholds, and bit error display operation, and 19 switch selectable clock rates between 1.2k and 12M bits/s. The unit is packaged as a self-contained 3.5" (8.89-cm) high rack mountable chassis. **Aydin Monitor Systems,** 401 Commerce Dr, Fort Washington, PA 19034.

Circle 258 on Inquiry Card

8-PORT MICROPROCESSOR BASED MULTIPLEXER

Allowing up to 8 asynchronous terminals to operate over a single synchronous line at up to 19.2k bits/s, the DE-8 Data Express is a microprocessor based multiplexer with terminal characteristics including terminal speeds selectable by port. Data accuracy is insured through ARQ, buffer memory, and data transparency. Key EIA leads plus unit status are reported on front panel LED indicator lights. The unit's character oriented transmission provides very short character processing time suitable for echoplex, faster ARQ operations, and minimal memory requirements. The operating program eases maintenance and allows software upgrades by permitting different software versions in paired units. An asynchronous network option allows the multiplexer to use asynchronous network facilities. This option allows for 14 different user selectable speeds from 50 to 9600 bits/s. **Compre Comm, Inc,** 51 E Chester St, Champaign, IL 61820.

Circle 259 on Inquiry Card

What price performance? Just $18K/Mbyte!

HP 1000 computers have always offered a great deal for the money. Now the deal is even more attractive.

Whether you choose the floating-point power of the F-Series, the high-speed E-Series, or the economical M-Series, you can fit the machine precisely to your job. And now you can do it with up to two megabytes of main memory for as little as $18K/Mbyte.

One month delivery!

The best part of the deal is that they're available now. With a 30-day delivery date, your system can be up and running while your competition is still waiting around.

It's no wonder you see so many HP 1000s in so many different engineering and manufacturing environments. With proven software for networking and data base management, upward-compatible RTE operating systems, a variety of I/O devices, and over 200 computer-compatible instruments for measurement and testing, the HP 1000 family offers high performance at a very down-to-earth price.

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Want to know them better? Just call your nearest HP office listed in the White Pages. Or fill out the coupon below, and we'll send you a free copy of our technical data manual.

HEWLETT hp PACKARD

I'd like to know more about HP 1000 computer systems. Please send me a free copy of your technical data manual.

My application is (system function)

For (type of company/industry)

Name Title

Company

Address

City State Zip

Phone

Mail to Hewlett-Packard
Attn: Roger Ueltzen
Dept. 1252,
11000 Wolfe Road,
Cupertino CA 95014

CIRCLE 128 ON INQUIRY CARD

NEW AUTUMN SCHEDULE

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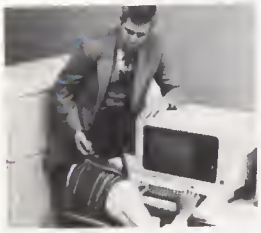
through cost-effective, Intensive Short Courses

Troubleshooting Microprocessor-Based Systems

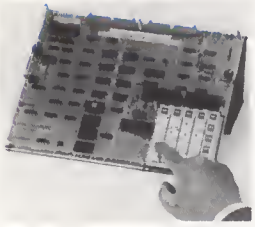


WASHINGTON, D.C. Oct. 15-19
NEW YORK Oct. 22-26
BOSTON Oct. 29-Nov. 2
PHILADELPHIA Nov 12-16
LOS ANGELES Dec. 10-14
SAN DIEGO Jan. 28-Feb. 1

Course 142 - Five days

This unique course is specifically designed for engineers and senior technicians involved in production testing, field service, and design of microprocessor-based systems. The course provides these personnel with the practical knowledge they require, including an in-depth understanding of: a) microprocessor software and hardware; b) how to apply the most powerful microprocessor debugging techniques; and c) how to use microprocessor troubleshooting equipment.

Microprocessor Hands-On Workshop



BOSTON Sept. 18-21
WASHINGTON, D.C. Sept. 25-28
NEW YORK Oct. 9-12
CLEVELAND Oct. 23-26
MINNEAPOLIS Oct. 30-Nov. 2
LOS ANGELES Nov. 13-16

Course 160 - Four days

This course is intended for engineers, programmers, systems analysts and their managers. It has been found extremely useful by attendees both with or without prior experience in either computers or electronics. In fact, managers who have attended report the course provides a level of familiarity, awareness, and confidence which enables them to better manage their staff in applying microprocessors.

EACH STUDENT RECEIVES A COMPLETE 8080 MICROCOMPUTER & INTERFACING SYSTEM FOR HIS PERSONAL USE THROUGHOUT THE COURSE.

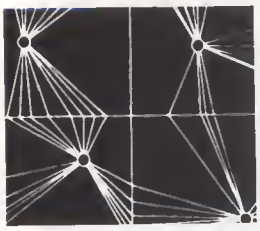
PASCAL: Programming in the Structured Language

WASHINGTON, D.C. Sept. 18-21
BOSTON Oct. 2-5
LOS ANGELES Oct. 9-12
NEW YORK Nov. 6-9
SAN FRANCISCO Nov. 13-16
SAN DIEGO Feb. 12-15

Course 330 - Four days

The PASCAL programming language is attracting widespread attention as a structured language tool for improving programmer productivity and reducing program maintenance costs. It is now being used both for implementing complex system programs and for applications ranging from commercial databases and word processing to scientific computations and instrument control. The course is designed for engineers, scientists, programmers, system analysts and their managers. THE COURSE INCLUDES HANDS-ON PROGRAMMING OF MICROCOMPUTERS IN PASCAL.

Distributed Processing and Computer Networks

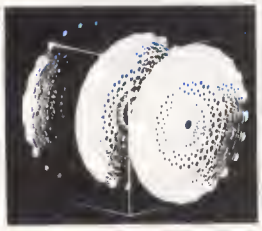


BOSTON Sept. 25-28
LOS ANGELES Oct. 9-12
WASHINGTON, D.C. Oct. 30-Nov.2
SAN DIEGO Jan. 22-25

Course 350 - Four days

This course provides a comprehensive introduction to distributed processing and computer network design techniques. It covers the individual elements of a distributed processing system and how these elements are synthesized to form a system which best meets application specific objectives. Throughout the course, application examples provide concrete examples of concepts presented, with emphasis on the factors affecting key planning, design and implementation decisions.

Computer Graphics State of the Art Techniques and Applications



BOSTON Sept. 18-21
WASHINGTON, D.C. Sept. 25-28
CHICAGO Oct. 9-12
NEW YORK Oct. 16-19
LOS ANGELES Oct. 30-Nov.2
SAN FRANCISCO Dec. 4-7

Course 365 - Four days

Hardware elements of computer graphics systems are presented at the level required for detailed system specification, selection and acquisition. Software techniques for computer graphic systems are developed from the elementary level of line generation and continue through advanced approaches to animated three-dimensional color displays with hidden surface removal. Off-the-shelf, commercially available software packages are analyzed and evaluated. Emphasis is placed on hardware/software tradeoffs, cost effectiveness and the advantages and limitations of alternative approaches.

TECHNOLOGY
from INTEGRATED COMPUTER SYSTEMS, INC.

INTEGRATED COMPUTER SYSTEMS, INC.

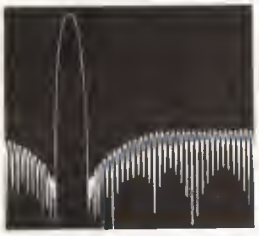
Digital Image Processing

WASHINGTON, D.C. Oct. 9-12
LOS ANGELES Dec. 11-14

Course 410 - Four days

This course is designed for programmers, analysts, engineers and scientists who need to acquire a fundamental knowledge of digital image processing techniques. The course provides the comprehensive mathematical and conceptual background necessary to design and implement systems for: image acquisition and display, analysis and measurement, enhancement and restoration, and coding and representation. Application areas will include military and aerospace systems, biomedical, remote sensing, earth resources, cartography, non-destructive testing and quality control.

Digital Signal Processing



WASHINGTON, D.C. Sept. 17-21
BOSTON Sept. 24-28
LOS ANGELES Oct. 15-19
CHICAGO Oct. 22 -26
SAN DIEGO Nov. 5-9
HOUSTON Jan. 21-25

Course 412 - Five days

The objective of this course is to present the necessary fundamentals of digital signal processing in a clear and comprehensive manner,to develop an understanding of new processing techniques, to survey the state of the art of hardware and software available, and to apply this information to a range of concrete design examples. The course is of benefit both for those who wish to achieve a basic understanding of this exciting area, and for those whose interest is in advanced techniques and the implementation of practical systems.

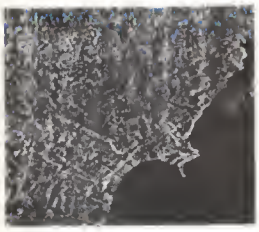
Fiber Optic Communication Systems

WASHINGTON, D.C. Sept. 18-21
LOS ANGELES Nov. 13-16
SAN FRANCISCO March 18-21

Course 440 - Four days

This course is designed for engineers, scientists and managers who are, or will be, involved in the planning, design and practical implementation of all types of communication systems. Commercially available components will be surveyed and concrete case studies of existing systems will be used to illustrate key managerial and technical considerations, emphasizing design techniques for the cost effective, practical application of this important technology.

Synthetic Aperture Radar Systems



WASHINGTON, D.C. Oct. 23-26
LOS ANGELES Nov. 13-16

Course 475 - Four days

The course provides an overview of SAR system design considerations; basic principles of operation; requirements on the antenna, transmitter-receiver, signal processor, display and motion compensation subsystems; and an exposition of image quality considerations. A quality evaluation model is developed which leads directly to the determination of detection probability for targets and terrain features. A concrete example SAR system will be designed and evaluated using a practical set of operational requirements.

ABOUT INTEGRATED COMPUTER SYSTEMS . . .

- These courses have been attended by over 15,000 engineers and managers worldwide
- Course Materials: 1000-1500 pages, including copies of all overhead transparencies as well as extensive reference materials
- Students praise the intense learning experience provided by expert instructors using an efficient multi-media audio/visual presentation
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300 N. Washington St., Suite 103
Alexandria, VA 22314
(703) 548-1333
WASHINGTON, D.C.

CIRCLE 129 ON INQUIRY CARD

PRODUCTS

IN-CIRCUIT PC BOARD TESTER

L527 assembly inspector, an in-circuit tester for locating and diagnosing assembly and component faults on analog, hybrid, and digital PC boards, consists of operator's test station and programming console. Test station includes microprocessor controlled test electronics, control panel for directing all system functions, work surface on which test fixture is placed, two tape drives, and thermal printer for generating hardcopy diagnostic error messages and fault summaries. Pins on user's test fixture are wired to test electronics by means of 40-pin ribbon cable connector on tester. In addition, a 14-pin IEH connector on tester interfaces test station with test fixture so that operator need only press start button on control panel for entire board handling test sequence to proceed automatically. **Teradyne, Inc,** 183 Essex St, Boston, MA 02111. Circle 260 on Inquiry Card

ERROR CORRECTING SINGLE-BOARD 64k MEMORY

Designed for DEC's PDP-11/34 minicomputer, NS11/34E has single 5-V power requirements and features single-bit error correct/multiple-bit error detect circuitry. Typ write access time is 100 ns, 50% faster than the MS11-L. Onboard error log can be interrogated in the maintenance mode via the 11/34's programmer console or similar I/O device. Malfunctioning RAMs can be identified and replaced at user's convenience. All RAMs are socketed for easy installation. A spare RAM is stored on the board. Byte level ECC permits byte level writes to be performed without additional internal memory cycles for proper ECC check bits. In event of multiple errors, ECC forces wrong parity. Memory can be operated with or in place of MS11-L series memories in DK11-CK, -DK, or -PK backplanes. **National Semiconductor Corp,** MS/7C265, 2900 Semiconductor Dr, Santa Clara, CA 95051.

3270 COMPATIBLE VIDEO DISPLAY TERMINAL

TC277-D is a downsize terminal that occupies approx 20% less physical space than conventional 3270 devices, yet incorporates features that increase both operator productivity and overall systems efficiency. Among these is an optional response time indicator that allows operators or supervisory staff to measure 4 different host CPU delays in responding to terminal transmissions. Measurements include response to last transmission, longest response, fastest response, and average response time for an operator selected group of past transmissions. Display is compatible with and operates under control of the company's TC371, 271, and 272 controllers as well as IBM model 3271 and 3272 controllers, and as a Level B device on IBM 3274 controllers. **Telex Terminal Communications,** 3301 Terminal Dr, Raleigh, NC 27604.
Circle 261 on Inquiry Card

★ In Half the Space ★ Up to 25% Savings ★

RX02-Compatible Double Density Floppies for the LSI-11/2

And Have it Your Way

With the LSI-11/2 built-in: The MF-211 Dual Floppy/LSI-11/2 does everything the 11V03-L will do . . .

The MF-211 Dual Floppy/LSI-11/2 System, using the CRDS Double Density Controller, is functionally identical to the DEC 11V03-L, but using only 10½" rack space. The MF-211 is the perfect low-cost answer to your 11V03-L requirement.

Check These Additional Features:

- Functionally identical to DEC's 11V03-L
- Double and Single Density Operation
- Complete Software/Media Compatibility with LSI-11/2
- Over One Megabyte Storage Per System
- Available with 4 Quad Slot or 8 Quad Slot Backplane
- DEC Software and Interface Cards available as options
- 30K Addressable Memory
- Considerable Dollar Savings

To go with your LSI-11/2: The FD-211 Dual Floppy System is the perfect plug replacement for your RX02 . . .

The FD-211 Double Density Floppy Disk System, using the CRDS Double-Density Controller, is totally software/media compatible with the Digital Equipment RX02 Floppy Disk System. It provides a compact, low-cost and highly reliable solution for all RX02 applications.

Check These Additional Features:

- 5¼" Low Profile Chassis
- Dual Shugart Drives
- 512K Bytes Per Drive
- Front Panel Write Protect Switches
- Photocell Write Protect
- Complete Instruction Manual

Why CRDS Products Give You So Much:

In addition to providing complete RX02 instruction set compatibility, the CRDS floppy disk controller card offers DMA data transfer by sector, bootstrap loader (eliminating need for DEC's REV-11 or BDV-11), IBM 3740 formatter, self-diagnostic, and interface electronics, all contained on a single dual-height card which plugs directly into the H9270 backplane. To design and package sophisticated controller electronics on a single dual-height card is a unique CRDS achievement, unmatched by any other controller supplier in the industry.

- RX02 Double Density and Single Density Operation
- Complete RX02 Software/Media Compatibility with LSI-11/2
- Integral Bootstrap Loader
- Built-In Self-Diagnostic, Formatter
- Dual-Height Controller for LSI-11 or LSI-11/2 Backplane

For more info on our FD-211 and MF-211 Double-Density Floppy Disk Systems, just call or write:

Charles River Data Systems, Inc.

4 Tech Circle, Natick, MA 01760 Tel. 617 655-1800 TWX 710 386 0523

CRDS

CIRCLE 131 ON INQUIRY CARD

SYNTHESIZED SIGNAL GENERATOR

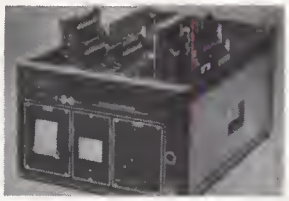
Using microprocessor control and keyboard entry of all functions, the model 380 retains all signal generator performance features of the 360, including the 20-μs switching speed attained through patented direct synthesis process, and frequency ranges from 10 kHz through 2000 MHz, with options to 4000 MHz. Additional features are digital readout of all functions, spin wheel tuning, function incrementing, frequency sweeping, and storage of up to 10 complete front panel setups. Noise floor is −138 dBc/Hz. Switching time is <20 μs within 0.1 radians of final phase at frequency. Remote programming of modes, range, and level is possible. External modulation input level is 1.0 Vrms at full scale. Other features include store/recall and sequence, learn mode, incrementing function values, digital sweep, frequency shift keying, and GPIB capability. **Ailtech, Div Cutler-Hammer,** 2070 Fifth Ave, Ronkonkoma, NY 11779.

Circle 262 on Inquiry Card

SERIES/1 FILE MANAGEMENT SYSTEM

Designed for IBM Series/1 with realtime programming system (RPS), RMS offers an integrated technique for data storage, retrieval, and manipulation with uniform directory utilization that enhances and simplifies RPS. The file management package offers efficient execution through effective management of all system resources. Sophisticated buffer management shares a single buffer pool for all system needs. Frequently used data are retained in fast memory. Record management ensures rapid access both sequentially and directly. Operating in the shared task set partition, the package is available to all users and user tasks. It is compatible with all versions of RPS and is used with assembler, COBOL, FORTRAN, and PL/1. During compilation, preprocessors convert all RMS commands to efficient source code with calls to the RMS runtime system. **Data Structures Inc,** 122 E 42nd St, New York, NY 10017.
Circle 263 on Inquiry Card

ONLINE COMPUTING DATA ACQUISITION AND REDUCTION SYSTEM



CompuDAS™ is a standalone microprocessor based instrument capable of functioning independently. Modular design enables users to configure specialized systems by adding plug-in cards. System interfaces to most types of electrical measurement devices via card subsystem. Analog and digital output as well as interfaces to a variety of front panel and peripheral accessories are provided. The system uses DABIL 1™ software, a version of Dartmouth BASIC. The basic system consists of portable or rackmounted chassis, all necessary power supplies, 18-slot card cage, microcomputer board, RAM board (16k expandable to 32k), DABIL 1 in P/ROM, and one RS-232 port (expandable to 5 ports). **Signal Laboratories, Inc,** 202 N State College Blvd, Orange, CA 92668.
Circle 264 on Inquiry Card

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⑥ **Computer Networks & Distributed Processing** — Burt H. Liebowitz	⑦ **Computer Communication Protocols** — John M. McQuillan	⑧ **Network Performance Analysis & Measurement** — Ira Richer & Peter Sevcik	⑨ **Computer Security & Integrity** — Dennis K. Branstad & Peter S. Browne	⑩ **Concurrent Pascal** — Kenneth Bowles
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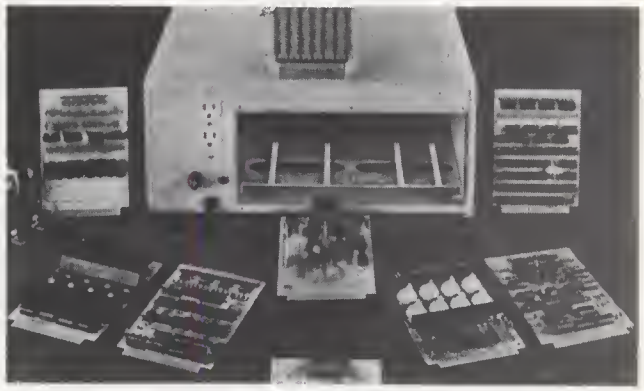
THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

DATA ACQUISITION/PROCESS CONTROL SYSTEM

Real World Interface System is a low cost, general purpose data acquisition and process control system designed for use with mini and microcomputers. Different plug-in modules give the user the flexibility and power to configure a system to meet needs. System cabinet includes a power supply, card cage, and motherboard with slots for up to 12 plug-ins. Plug-in modules include A-D and D-A converters, and a computer interface card. Each plug-in card has at least 8 channels of input or output (except for a max of 4 channels on the current probe); some have 16 or 32 channels. All plug-ins can be obtained in kit form or assembled and tested. The cabinet is complete with motherboard, power supply, and parallel CPU interface. **General Computer Technology,** 400 S Lipan, Suite 2, Denver, CO 80223.



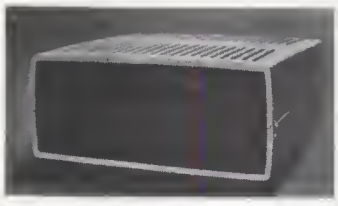
Circle 265 on Inquiry Card

BLIS/COBOL MULTIUSER OPERATING SYSTEMS

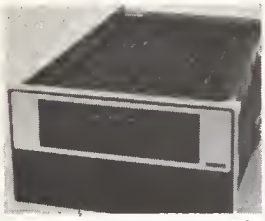
Communications options contained in 3.2 Version of BLIS/COBOL operating system include Inter Branch (BLIS to BLIS), IBM bisync point-to-point, Burroughs TC500, IBM 2780, 3780, and 3270 with operations such as switched or multipoint (with BLIS/COBOL either being polled or doing the polling), ASCII or EBCDIC data, and transparent or non-transparent modes. Communications options support half-duplex lines with modem control or full-duplex lines with or without modem control at speeds from 110 through 9600 baud. Lines can be dedicated or dial-up with or without auto-answer. Up to 3 simultaneous communications lines may be operational using the same or different line disciplines concurrent with other multiuser COBOL program activity. The system runs on various mainframes and provides support for miniperipherals. **Information Processing Inc,** 1850 Lee Rd, Winter Park, FL 32789. Circle 266 on Inquiry Card

STANDALONE COMMUNICATIONS TAPE TERMINAL

Dual-port microprocessor controlled tabletop tape terminals series 1000 are based on dual 3M Co DC100 tape cartridge storage, provide 672k bytes of unformatted capacity, and incorporate RS-232 interfaces for receiving/transmitting digital data over telephone lines and other communications links. Handling variable data transmission rates up to 9600 baud, the units can be controlled from front panel pushbuttons, or placed under full remote control. Remote control permits operation from a nearby CRT terminal or other keyboard, or alternatively from a distant computer or centralized facility. Tape transports incorporate read-after-write heads plus CRC to ensure error free operations. Additional standard communications functions also include store/forward, batch processing, and data storage. **Qantex Div, North Atlantic Industries, Inc,** 60 Plant Ave, Hauppauge, NY 11787. Circle 267 on Inquiry Card



MICROPROCESSOR BASED, 9-CHANNEL PARALLEL CONTROLLER

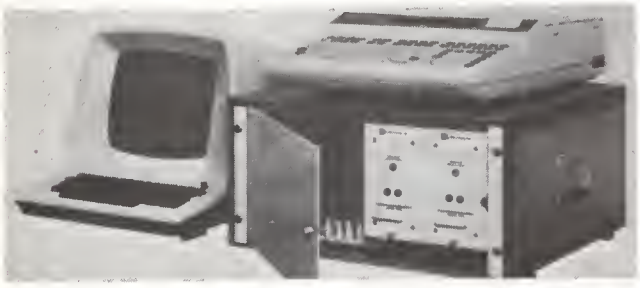


Designed to interface with PTD-9309 parallel transfer disc drives, the DCP-909 controller offers data transfer rate of 87.1M bits/s, and provides control for up to 4 disc drives with total unformatted storage capacity of up to 1248M bytes. Controller can record or play back data on a single set of 8 or 9 vertically aligned sectors that can be accessed concurrently through 1 of 2 disc system 9-head groups. It is equipped with disc interface, 4 FIFO memory buffers, high speed parallel data interface, host interface, and bit-slice microprocessor to control sequence of operations required to execute requests from host minicomputer. Disc interface provides high speed control and timing signals required to record or play back data to or from disc drives and adds necessary sync and CRC bits to each sector. Initial units will interface with DEC PDP-11 series computers. **Ampex Corp,** 401 Broadway, Redwood City, CA 94063. Circle 268 on Inquiry Card

SOFTWARE PACKAGE FOR X.25 PACKET SWITCHED NETWORK PROTOCOL

Supplied as part of Guardian operating system, AXCESS package allows the company's NonStop™ computer systems to communicate directly over public packet switched networks using std protocols defined for use with X.25. Included are protocols that allow access to virtually any computer or terminal. Interactive terminal interface provides for remote terminal access to host system from anywhere. Remote terminals look like local terminals with no special programming necessary. In addition, package allows application within system to communicate with any other data terminal equipment connected to packet network using any agreed upon protocol. An additional higher level protocol is used to permit distributed systems to be linked together through a public packet network using the EXPAND software. **Tandem Computers, Inc,** 19333 Vallco Pkwy, Cupertino, CA 95014.
Circle 269 on Inquiry Card

IEEE-488 COMPATIBLE INPUT CONDITIONING SYSTEM



Measurement and control system is completely IEEE-488 compatible and is designed to interface with most desktop calculators. A-D isolation via an optical transceiver minimizes noise interference and provides high common mode immunity; a programmable reference supply with NBS traceability is provided. Integral signal conditioning with std 6-wire configuration and R-CAL are also offered. Acquisition expansion to 2000 channels, automatic bridge balancing, and integral discrete I/O and DAC output for process control are accommodated. Basic system includes chassis, power supply, and various signal conditioning cards. Available in rack-mountable or desktop configuration, max chassis capacity is 128 channels. Each chassis accommodates 4 types of plug-in cards: signal conditioning multiplexer, voltage input/multiplexer, DAC, and discrete I/O cards. **Cyber Systems, Inc,** 2031 E Cerritos Ave, Anaheim, CA 92806.
Circle 270 on Inquiry Card

LITERATURE

Schottky Power Rectifiers

Series of three data sheets features listings of mechanical, electrical, and thermal operating characteristics; engineering line drawings; and performance charts for series 030, 060, and F230 rectifiers. **FMC Corp, Semiconductor Products Div,** Broomfield, Colo.
Circle 300 on Inquiry Card

Flexible PCB Jumpers

Catalog supplies specs including pitch, length, thickness, pin dia, number of conductors, insulation material, and pin arrangement for Flexstrip jumpers that bridge circuit boards. **T&B/Ansley Corp,** Los Angeles, Calif.
Circle 301 on Inquiry Card

Signal Processing Equipment

Brochure describes functional units of signal processor, outlines software support, and lists governmental, industrial, research, and telecommunications applications. **Signal Processing Systems, Inc,** Waltham, Mass.
Circle 302 on Inquiry Card

Microprocessor Controlled Voice Response

A 4-p bulletin presents 680 series microprocessor controlled, solid state voice response Speechmaker that uses natural word length and any language vocabulary. **Cognitronics Corp,** Stamford, Conn.
Circle 303 on Inquiry Card

Dual-Channel FFT Analyzer

Application oriented brochure describing 660A dual-channel FFT realtime spectrum analyzer focuses on nine problems the analyzer solves including how to choose the most meaningful form of processing. **Nicolet Scientific Corp,** Northvale, NJ.
Circle 304 on Inquiry Card

COBOL 74

Containing the latest information relative to X3.23-1974 (COBOL 74), bulletin #18 produced by ANS Technical Committee includes 107 interpretations. To order a copy, send check for $6.50 made payable to CBEMA to CIB #18, X3 Secretariat, **CBEMA,** 1828 L St, NW, Suite 1200, Washington, DC 20036.
Circle 305 on Inquiry Card

16-Bit Microcomputer Modules

Selection guide and catalog includes specs and descriptions that reference TM990 series modules, software, firmware, and hardware products. **Texas Instruments, Inc,** Houston, Tex.
Circle 306 on Inquiry Card

Intelligent Port Selector

Introducing model 610 intelligent port selector, brochure includes functional description and specs. **Micom Systems, Inc,** Chatsworth, Calif.
Circle 307 on Inquiry Card

Keyless Digital Lock

Brochure cites specs, timing diagram, logic flowchart, block diagram, and typ applications for monolithic, ion-implanted PMOS 4-digit lock. **LSI Computer Systems, Inc,** Melville, NY.
Circle 308 on Inquiry Card

Indicator Lights

Catalog and technical manual describe LED, relampable, and non-relampable lights with photos, dimension drawings, mounting information, specs, and ratings. **Industrial Device, Inc,** Edgewater, NJ.
Circle 309 on Inquiry Card

Integrated Circuits

CMOS/LSI, MOS/LSI, CMOS, memory microsystem, data acquisition, linear, discrete, and hybrid/analog gate devices are profiled with specs in condensed product guide. **Intersil, Inc,** Cupertino, Calif.
Circle 310 on Inquiry Card

Fiber Optics Cable

Brochure provides cross-section drawings, fiber specs, attenuation and response charts, and tables of physical characteristics for 1-, 2-, 6-, and 18-fiber cable. **Belden Corp,** Geneva, Ill.
Circle 311 on Inquiry Card

Digital Plotting System

CPS-11, that combines 4000-step/s digital plotter and microprocessor based controller and has engineering and business applications, is described in literature. **Houston Instrument Div of Bausch and Lomb,** Austin, Tex.
Circle 312 on Inquiry Card

Subminiature Toggle and Pushbutton Switches

Electrical and materials specs, switching functions, photos, and actual size mechanical outlines are presented in catalog covering 40 lines of switches. **American Switch Corp,** Wakefield, Mass.
Circle 313 on Inquiry Card

Bus Bars and Clip Buses

Standard and custom designs for solderless clip bus, single and multiconductor vertical bus bars, and for bus that fits under DIPs are profiled with specs in brochure. **Logic Dynamics Inc,** Gardena, Calif.
Circle 314 on Inquiry Card

Monopanel Touch Switches

Designers' guide outlines method of operation, construction, terminations, mounting, audio and visual feedback, dimensions, graphics, and prototyping panels for switch systems. **Centralab Electronics Div, Globe-Union Inc,** Milwaukee, Wis.
Circle 315 on Inquiry Card

Closed Loop Positioning Module

Specs and interconnection diagram for servo drive/digital control package that interfaces with programmable controllers, as well as other control systems, are supplied in spec sheet. **Hyper-loop Inc,** Bridgeview, Ill.
Circle 316 on Inquiry Card

High Voltage Power Supplies

Technical information, applications, and dimensions are included in catalog featuring laboratory, multiple output CRT, ac and dc input modules, and electron beam power supplies. **Bertan Associates, Inc,** Syosset, NY.
Circle 317 on Inquiry Card

Permanent Magnet Servomotors

Catalog includes motor selection information, electrical specs, schematics, performance curves, dimensional drawings, and photos for ceramic, Alnico, and rare earth servomotors. **Clifton Precision, Litton Systems, Inc,** Clifton Heights, Pa.
Circle 318 on Inquiry Card

ASCII Display Terminal

Data sheet lists specs, std functions, operating modes, applications support, features, and options of concept 100 CRT display and keyboard. **Human Designed Systems, Inc,** Philadelphia, Pa.
Circle 319 on Inquiry Card

Punched Card and Badge Reader

Operation of heavy duty serial and static parallel punched card and badge readers is described in catalog; specs, dimensional drawings, and photos are also supplied. **Taurus Corp,** Lambertville, NJ.
Circle 320 on Inquiry Card

RF Connectors

Catalog lists ConheX connector line incorporating SMB, SMC, and Slide-On interfaces, and contains detailed electrical and mechanical specs. **Sealectro Corp,** Mamaroneck, NY.
Circle 321 on Inquiry Card

Battery Chargers and Charging

Handbook cites brief history, discusses battery chargers, and evaluates current technologies including regulation, current limiting, and fast charging. **Ratelco, Inc,** Seattle, Wash.
Circle 322 on Inquiry Card

Regulated dc Power Subassemblies

Performance specs, operational data charts, and design examples for LSS series subassemblies that rectify, filter, and regulate are included in brochure. **Lambda Electronics,** Melville, NY.
Circle 323 on Inquiry Card

6-Channel Recorder

Potentiometric Miniservo[R] recorder with two, four, or six pens is described with specs and dimensions in brochure. **Esterline Angus Instrument Corp,** Indianapolis, Ind.
Circle 324 on Inquiry Card

Automotive Electronics

Product guide groups by applications components needed to build engine management systems, entertainment features, instrumentation, safety, comfort, and convenience devices. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95951.

Switching Power Supplies

Catalog furnishes ratings, specs, dimensional drawings, and photos for S series single-, dual-, triple-, and quad-output, open and closed frame supplies. **Deltron Inc,** North Wales, Pa.
Circle 325 on Inquiry Card

Mass Termination System

Jaguar wire to post interconnect system for discrete wire or ribbon cable, plus application tooling are featured in catalog that includes photographs, selection charts, and dimension drawings. **Methode Electronics, Inc,** Rolling Meadows, Ill.
Circle 326 on Inquiry Card

Microprocessor Based Cassette Terminal

Brochure supplies operating features, specs, and photos of microprocessor based digital cassette data terminal family. **MFE Corp,** Salem, NH.
Circle 327 on Inquiry Card

Torque Motors

Current issue of *Motorgram* contains selection information for torque motors plus application case history of x-ray pipeline welders propelled by company's gearmotors. **Bodine Electric Co,** Chicago, Ill.
Circle 328 on Inquiry Card

Data Communication Test Equipment

Detailing line of digital test and monitoring equipment, 166-p catalog presents technical specs, illustrations, and applicational configurations. **International Data Sciences, Inc,** Lincoln, RI.
Circle 329 on Inquiry Card

Microcomputer Products

Wallchart size flyer describes line of MULTIBUS compatible hardware and software products. **Monolithic Systems Corp,** Englewood, Colo.
Circle 330 on Inquiry Card

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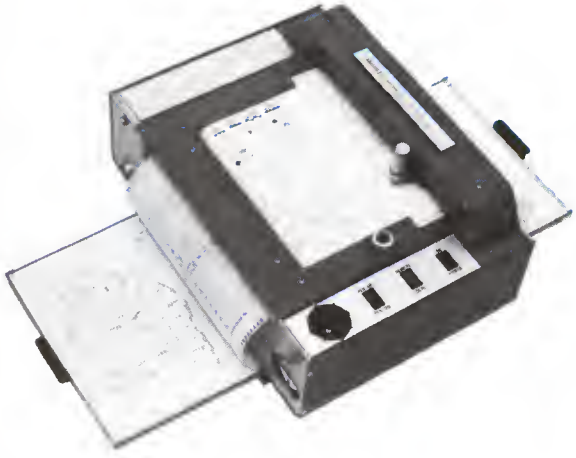

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